PROJECT 802 LOCAL & METROPOLITAN AREA NETWORKS

DRAFT SUPPLEMENT TO IEEE STD 1802.3-1991
CONFORMANCE TEST METHODOLOGY FOR CSMA/CD ACCESS METHOD
AND PHYSICAL LAYER SPECIFICATIONS

10BASE-T MAU CONFORMANCE TESTING (SECTION 6)

Draft 7C

Draft 7C is a result of the changes made at the Denver, CO meeting July 12-16, 1993 by the 10BASE-T Conformance Test Sub-Task Force. It consists of minor editorial changes based on feedback from TCCC confirmation ballot comments and final editorial review of draft 7. This draft expires August 31, 1993 or earlier if superseded by another draft.

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Revisions to IEEE Std 1802.3-1991

(These changes and additions are part of P1802.3d-199X.)

The following changes add references and abbreviations used by or referred to in 10BASE-T Conformance Testing (chapter 6) to the appropriate places in IEEE Std 1802.3-1991.

1.3 Acronyms and Abbreviations

Add these acronyms and abbreviations to the list:

AWG	Arbitrary Waveform Generator
BAL	Balanced-Unbalanced Matching Transformer (Balun)
BT	Bit Time
CP	Current Probe
DP	Differential Probe
FG	Function Generator
HDP	High Performance DIfferential Probe
IDL	Idle Signal
IUT	Implementation Under Test
LTPG	Link Test Pulse Generator
MDI	Medium Dependent Interface
RD	Receive Data
SFD	Start Frame Delimiter
SOI	Start Of Idle
SQE	*signal_quality_error*
TD	Transmit Data
TPG	Test Pattern Generator
TPM	Twisted Pair Model

1.8 References

Add these references to the list of references:

[6] IEEE Std. 802.3i-1990 (Supplement to ISO/IEC 8802-3:1992/ANSI/IEEE Std 802.3-1992 Edition) [ISO/IEC 8802-3:1992, DAM9].

[7] IEEE Std. 802.3l-1992 , Type 10BASE-T PICS Proforma (Supplement to ISO/IEC 8802-3:1992/ANSI/IEEE Std 802.3-1992 Edition) [ISO/IEC 8802-3:1992, PDAM17]

[8] IEC Publication 60, High-voltage test techniques.

[9] IEC Publication 950, Safety of Information Technology Equipment, Including Electrical Business Equipment.

6. 10BASE-T MAU Conformance Testing

6.1 Scope of 10BASE-T MAU Conformance Test. The purpose of this section is to define abstract methods for the conformance testing of 10BASE-T MAU implementations in order to satisfy conformance requirements arising from the P802.3i [6] 10BASE-T MAU specification. Such methods will form the basis for any subsequent development of executable test cases. This document is applicable to the conformance testing of CSMA/CD 10BASE-T MAU, hereafter referred to as MAU, implementations that have been designed to section 14 of P802.3i [6]. Additional information about the implementation under test may be found in the PIXIT.

6.1.1 Embedded MAUs. Many of these tests do not apply to embedded MAUs where the physical AUI does not exist. In those cases, other standards may apply.

6.2 10BASE-T MAU Abstract Test Suite. This is comprised of one category of test groups. The category relates to capability testing. Within this category are a number of test groups, where each group is aimed at collecting individual test cases together that share some commonality in features tested or test methods used. The MAU test method is Local Single as per ISO 9646 [2]. The format for the test case headers follows the outline of Section 1.5, with the addition of a “PICS Reference:” line that cross-references the test case to a particular section/item of IEEE Std. 802.3l-1992 [ISO/IEC 8802-3:1992, PDAM17] [7].

Test Suite ID	:	1411
Test Suite Name	:	10BASE-T MAU Abstract Tests
Applicable Standards	:	ISO 8802-3:1992 [3] IEEE Std 802.3i-1990 [ISO/IEC 8802-3:1992, DAM9] [6]
OSI RM Layer	:	Physical
OSI RM Sublayer	:	Medium Attachment Unit (MAU)
Class or Access	:	CSMA/CD
Transmission Type	:	10BASE-T
Purpose	:	To assess conformance of the physical interface to applicable standards.
General Setup	:	Unless otherwise stated in individual test procedures, all tests shall start with “Apply power to the MAU and bring the MAU into Link Test Pass State.” In addition, all tests requiring the application of power to the MAU via the AUI shall be performed with 11.28 V applied through a 3.5 Ω 1% resistor to the VP circuit of the MAU and with 15.75 V applied through no series resistor to the VP circuit of the MAU, unless otherwise stated. For both voltage levels, all stray wiring and connection resistance for both the VP circuit and the VC circuit combined shall be limited to a maximum of 0.405 Ω excluding the resistance of conformant AUI connector connections at the source and MAU ends. All AUI applied voltages are with reference to circuit VC. When required, the MAU can be verified to be in a Link Test Fail state by monitoring the DI circuit for *input_idle* messages and the TD circuit for *TD_idle* messages.

6.2.1 Capability and Behavior Tests

6.2.1.1 Test Group 1411.01 - Transmit Functions

Test Group ID	:	1411.01
Test Group Name	:	Transmit Functions.
Test Group Purpose	:	To verify the characteristics of the Transmit Function.

Test Case ID	:	1411.01.01
Test Case Name	:	Transmit signal polarity.
Status	:	MANDATORY
Standard Reference.	:	14.2.1.1
PICS Reference	:	14.10.4.5.2/1, 14.10.4.5.2/2
History	:	
Test Purpose	:	To verify the polarity of the TD circuit signals in relation to the DO circuit signals.
Note	:	
Test Setup	:	Test setup B.
Test Procedure	:	Apply test signal 1 to the DO circuit of the MAU. Monitor the DO circuit and the TD circuit for correct logical sense after the initial bit loss time and before the start of idle of a packet transmission.
Conformance	:	The MAU shall receive the signals on the DO circuit and send them to the TD circuit of the MDI. A positive signal on the A lead relative to the B lead of the DO circuit shall result in a positive signal on the TD+ (Transmit Data +) lead of the MDI with respect to the TD- lead.

Test Case ID	:	1411.01.02
Test Case Name	:	Transmit start-up bit loss.
Status	:	MANDATORY
Standard Reference	:	14.2.1.1
PICS Reference	:	14.10.4.5.2/3
History	:	
Test Purpose	:	To verify the number of bits received on the DO circuit and not transmitted on the TD circuit.
Note	:	
Test Setup	:	Test setup B.
Test Procedure	:	Apply test signal 1 to the DO circuit of the MAU. Monitor the DO circuit and TD circuit. Measure the number of bits received on the DO circuit and not transmitted onto the TD circuit using the Start Frame Delimiter (SFD) for reference.
Conformance	:	At the start of a packet transmission, no more than 2 bits may be received by the MAU from the DO circuit and not transmitted on the TD circuit. It is permissible for the first bit sent to contain phase violations or invalid amplitude.

Test Case ID	:	1411.01.03
Test Case Name	:	Transmit settling time.
Status	:	MANDATORY
Standard Reference	:	14.2.1.1
PICS Reference	:	14.10.4.5.2/4
History	:	
Test Purpose	:	To verify the timing and signal level of the second bit cell transmitted.
Note	:	
Test Setup	:	Test setup B.
Test Procedure	:	Apply test signal 1 to the DO circuit of the MAU. Monitor the DO circuit and TD circuit. Observe the second and subsequent

		bits on the TD circuit.
Conformance	:	The second bit transmitted on the TD circuit shall be transmitted with the correct timing and signal levels.

Test Case ID	:	1411.01.04
Test Case Name	:	Transmit steady state delay.
Status	:	MANDATORY
Standard Reference	:	14.2.1.1
PICS Reference	:	14.10.4.5.2/5
History	:	
Test Purpose	:	To verify the propagation delay between the DO circuit and the TD circuit.
Note	:	
Test Setup	:	Test setup B.
Test Procedure	:	Apply test signal 1 to the DO circuit of the MAU. Monitor the DO circuit and TD circuit. Measure the propagation delay from a bit's zero crossing on the DO circuit to the corresponding bit's zero crossing on the TD circuit using the SFD for reference.
Conformance	:	The steady state propagation delay between the DO circuit input and the TD circuit shall not exceed 2 bit times.

Test Case ID	:	1411.01.05
Test Case Name	:	Transmit delay variability.
Status	:	MANDATORY.
Standard Reference	:	14.2.1.1
PICS Reference	:	14.10.4.5.2/6
History	:	
Test Purpose	:	To verify the start-up delay variability between two packets.
Note	:	
Test Setup	:	Test setup B.
Test Procedure	:	Apply test signals 2a-f to the DO circuit of the MAU. Monitor the DO circuit and TD circuit. Measure the start-up delay (bit loss plus steady state propagation delay) for a packet and the subsequent packet. Repeat the test 100 times to determine the largest variability.
Conformance	:	For any two packets that are separated by 9.6 µs or less, the start-up delay (bit loss plus steady-state propagation delay) of the first packet shall not exceed that of the second packet by more than 2 bit times.

Test Case ID	:	1411.01.06
Test Case Name	:	TP_IDL, silence duration and silence voltage.
Status	:	MANDATORY
Standard Reference	:	14.2.1.1
PICS Reference	:	14.10.4.5.2/7, 14.10.4.5.2/8
History	:	
Test Purpose	:	To verify the timing of the TP_IDL signal.
Note	:	
Test Setup	:	Test setup B.
Test Procedure	:	Apply test signal 1 to the DO circuit of the MAU. Monitor the TD circuit. Measure the period of silence between the start of

		TP_IDL and the link test pulse. Measure the time between repeating link test pulses.
Conformance	:	Whenever data is not being transmitted on the TD circuit, an idle signal, TP_IDL, shall be transmitted on the TD circuit. TP_IDL is a start of idle as defined in 14.3.1.2.1 followed by a repeating sequence of a 16 ± 8ms period of silence (the time where the differential voltage remains at 0 ± 50 mV) and a link test pulse (see 14.3.1.2.1).

Test Case ID	:	1411.01.07
Test Case Name	:	TP_IDL signal termination with respect to start of packet and link test pulse.
Status	:	MANDATORY
Standard Reference	:	14.2.1.1
PICS Reference	:	14.10.4.5.2/9
History	:	
Test Purpose	:	To verify correct termination of the TP_IDL signal.
Note	:	*This test case is considered untestable. It is not practical to measure and is not considered critical. Even though testing for compliance is not practical, conformance to the standard,* ***by design*** *, is the responsibility of the manufacturer with compliance status to be noted in the PICS.*
Test Setup	:	
Test Procedure	:	
Conformance	:	Transmission of TP_IDL may be terminated at any time with respect to the link test pulse. It shall be terminated such that no more than the first transmitted bit of a packet is corrupted and with no more delay than is specified for bit loss and steady-state propagation.

6.2.1.2 T est Group 141 1.02 - Receive Functions

Test Group ID	:	1411.02
Test Group Name	:	Receive Functions.
Test Group Purpose	:	To verify the characteristics of the Receive Function.

Test Case ID	:	1411.02.01
Test Case Name	:	Receive start-up bit loss.
Status	:	MANDATORY
Standard Reference	:	14.2.1.2
PICS Reference	:	14.10.4.5.3/3
History	:	
Test Purpose	:	To verify the number of bits received on the RD circuit and not transmitted on the DI circuit.
Note	:	
Test Setup	:	Test setup L.
Test Procedure	:	Apply test signal 1 to the DO circuit of the tester MAU. Monitor the RD circuit and DI circuit on the MAU under test. Measure the number of bits received on the RD circuit of the MAU under test and not transmitted on the DI circuit of the MAU under test using the SFD for reference.
Conformance	:	At the start of a packet reception from the RD circuit, no more

than 5 bits may be received from the RD circuit and not transmitted onto the DI circuit.

Test Case ID	:	1411.02.02
Test Case Name	:	Receive steady state delay.
Status	:	MANDATORY
Standard Reference		14.2.1.2
PICS Reference	:	14.10.4.5.3/5
History	:	
Test Purpose	:	To verify the propagation delay from the RD circuit to the DI circuit.
Note	:	
Test Setup	:	Test setup L.
Test Procedure	:	Apply test signal 1 to the DO circuit of the tester MAU. Monitor the DI circuit and RD circuit on the MAU under test. Measure the propagation delay between a bit's zero crossing on the RD circuit of the MAU under test and the corresponding bit's zero crossing on the DI circuit of the MAU under test using the SFD for reference.
Conformance	:	The steady-state propagation delay between the RD circuit and the DI circuit shall not exceed 2 bit times.

Test Case ID	:	1411.02.03
Test Case Name	:	Receive signal polarity.
Status	:	MANDATORY
Standard Reference	:	14.2.1.2
PICS Reference	:	14.10.4.5.3/1, 14.10.4.5.3/2
History	:	
Test Purpose	:	To verify the polarity of the DI circuit signals in relation to the RD circuit signals.
Note	:	
Test setup	:	Test setup L
Test Procedure	:	Apply test signal 1 to the DO circuit of the tester MAU. Monitor the DI circuit and RD circuit signals on the MAU under test for correct logical sense after the initial bit loss time and before the start of idle of the packet.
Conformance	:	The MAU shall receive the signals on the RD circuit of the MDI and send them to the DI circuit. A positive signal on the RD+ (Receive Data +) lead relative to the RD- lead of the MDI shall result in a positive signal on the A lead with respect to the B lead of the DI circuit.

Test Case ID	:	1411.02.04
Test Case Name	:	Receive delay variability.
Status	:	MANDATORY
Standard Reference	:	14.2.1.2
PICS Reference	:	14.10.4.5.3/6
History	:	
Test Purpose	:	To verify the start-up delay between two packets.
Note	:	
Test Setup	:	Test setup H.

Test Procedure : Apply test signals 24a-f to the RD circuit of the MAU under test. Monitor the DI circuit and RD circuit signals. Measure how much the start-up delay (bit loss plus steady-state propagation delay) exceeds the delay of the subsequent packet. Repeat the test 100 times and note the worst case value.

Conformance : For any two packets that are separated by 9.6 us or less, the start-up delay (bit loss plus steady-state propagation delay) of the first packet shall not exceed that of the second packet by more than 2 bit times.

Test Case ID : 1411.02.05
Test Case Name : Receive settling time.
Status : MANDATORY
Standard Reference : 14.2.1.2
PICS Reference : 14.10.4.5.3/4
History :
Test Purpose : To verify the timing and signal level of the second bit transmitted.
Note :
Test Setup : Test setup L.
Test Procedure : Apply test signal 1 to the DO circuit of the tester MAU. Monitor the DI circuit and RD circuit on the MAU under test. Observe the second and subsequent bits on the DI circuit of the MAU under test.
Conformance : It is permissible for the first bit sent on the DI circuit to contain phase violations or invalid data; however all successive bits of the packet shall be sent with no more than the amount of jitter specified in 14.3.1.3.1.

6.2.1.3 Test Group 1411.03 - Loopback Functions

Test Group ID : 1411.03
Test Group Name : Loopback Functions.
Test Group Purpose : To verify the functional characteristics of the Loopback Function.

Test Case ID : 1411.03.01
Test Case Name : Loopback function when RD = idle and DO = active.
Status : MANDATORY
Standard Reference : 14.2.1.3
PICS Reference : 14.10.4.5.4/1
History :
Test Purpose : To verify the Loopback function requirements when RD is idle and DO is active.
Note :
Test Setup : Test setup B.
Test Procedure : Apply test signal 1 to the DO circuit of the MAU. Monitor the DI circuit.
Conformance : When the MAU is transmitting on the TD circuit and is not receiving *RD_input* messages on the RD circuit, the MAU shall transmit on the DI circuit the signals received on the DO circuit in order to provide loopback of the transmitted signal.

Test Case ID	:	1411.03.02
Test Case Name	:	Loopback bit loss (DO to DI circuits).
Status	:	MANDATORY
Standard Reference	:	14.2.1.3
PICS Reference	:	14.10.4.5.4/2
History	:	
Test Purpose	:	To verify the number of bits transmitted on the DO circuit and not received on the DI circuit.
Note	:	
Test Setup	:	Test setup B.
Test Procedure	:	Apply test signal 1 to the DO circuit of the MAU. Monitor the DI circuit and DO circuit. Measure the number of bits received on the DO circuit and not transmitted on the DI circuit using the SFD for reference.
Conformance	:	At the start of a packet transmission on the TD circuit, no more than 5 bits of information may be received from the DO circuit and not transmitted to the DI circuit.

Test Case ID	:	1411.03.03
Test Case Name	:	Loopback steady state delay.
Status	:	MANDATORY
Standard Reference	:	14.2.1.3
PICS Reference	:	14.10.4.5.4/4
History	:	
Test Purpose	:	To verify the propagation delay from the DO circuit to the DI circuit.
Note	:	
Test Setup	:	Test setup B.
Test Procedure	:	Apply test signal 1 to the DO circuit of the MAU. Monitor the DI circuit and DO circuit. Measure the propagation delay from a bit's zero crossing on the DO circuit to the corresponding bit's zero crossing on the DI circuit using the SFD for reference.
Conformance	:	The steady-state propagation delay between the DO circuit and the DI circuit shall not exceed 1 BT.

Test Case ID	:	1411.03.04
Test Case Name	:	Loopback settling time.
Status	:	MANDATORY
Standard Reference	:	14.2.1.3
PICS Reference	:	14.10.4.5.4/3
History	:	
Test Purpose	:	To verify the timing and signal level of the second bit cell transmitted.
Note	:	
Test Setup	:	Test setup B.
Test Procedure	:	Apply test signal 1 to the DO circuit of the MAU. Monitor the DI circuit and DO circuit signals. Observe the second and subsequent bits of the DI circuit data.
Conformance	:	It is permissible for the first bit sent on the DI circuit to contain phase violations or invalid data; however all successive bits of

the packet shall meet the jitter specified in 14.3.1.3.1 (that is 13.5 ns plus 1.5 ns).

6.2.1.4 Test Group 1411.04 - Collision Functions

Test Group ID : 1411.04
Test Group Name : Collision Functions.
Test Group Purpose : To verify the functional characteristics of the Collision Function.

Test Case ID : 1411.04.01
Test Case Name : No collision state.
Status : MANDATORY
Standard Reference : 14.2.1.4
PICS Reference : 14.10.4.5.5/4
History :
Test Purpose : To verify the presence and the signal characteristics of IDL on the CI circuit when there is no collision, SQE test or jabber.
Note :
Test Setup : Test setup M.
Test Procedure : Monitor the CI circuit of the MAU under test.

(1) Apply test signal 1 to the DO circuit of the tester MAU and IDL to the DO circuit of the MAU under test.
(2) Apply test signal 1 to the DO circuit of the MAU under test and IDL to the DO circuit of the tester MAU.

Verify that CI is asserting IDL while DI is active.

Conformance : The signal present on the CI circuit in the absence of a collision, SQE test, or jabber shall be the IDL signal.

Test Case ID : 1411.04.02
Test Case Name : Collision state.
Status : MANDATORY
Standard Reference : 14.2.1.4
PICS Reference : 14.10.4.5.5/1
History :
Test Purpose : To verify the presence and the signal characteristics of CS0 on the CI circuit when there is a collision.
Note :
Test Setup : Test setup O.
Test Procedure : Monitor the CI circuit, DO circuit, and TD circuit of the MAU under test.

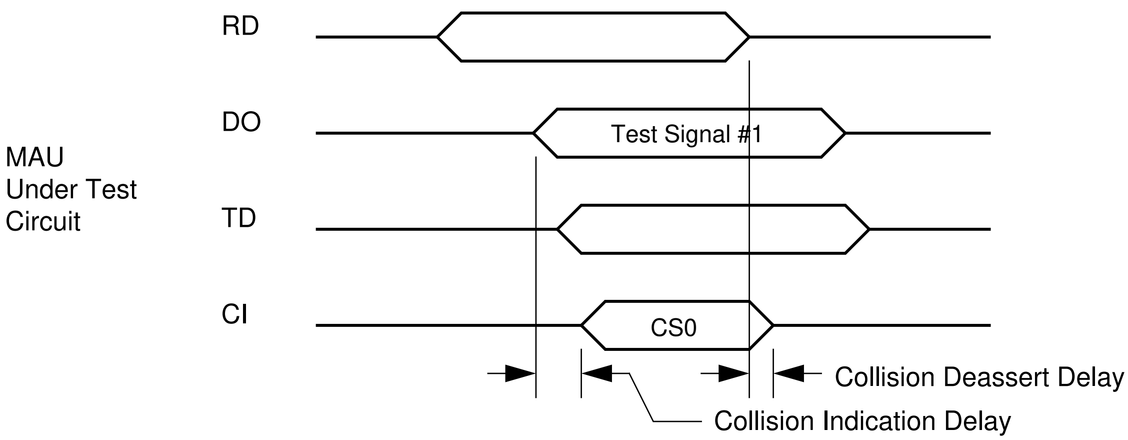
(1) Apply test signal 1 to the DO circuit of the tester MAU. Apply test signal 1 to the DO circuit of the MAU under test to create a collision. Verify on the MAU under test that the signals on the DO circuit appear on the TD circuit and that CS0 is present on the CI circuit (see Fig 6-1a).
(2) Apply test signal 1 to the DO circuit of the MAU under test. Apply test signal 1 to the DO circuit of the tester MAU to create a collision. Verify on the MAU under test that the signals on the DO circuit appear on the TD circuit and that CS0 is present on the CI circuit (see Fig

6-1b).

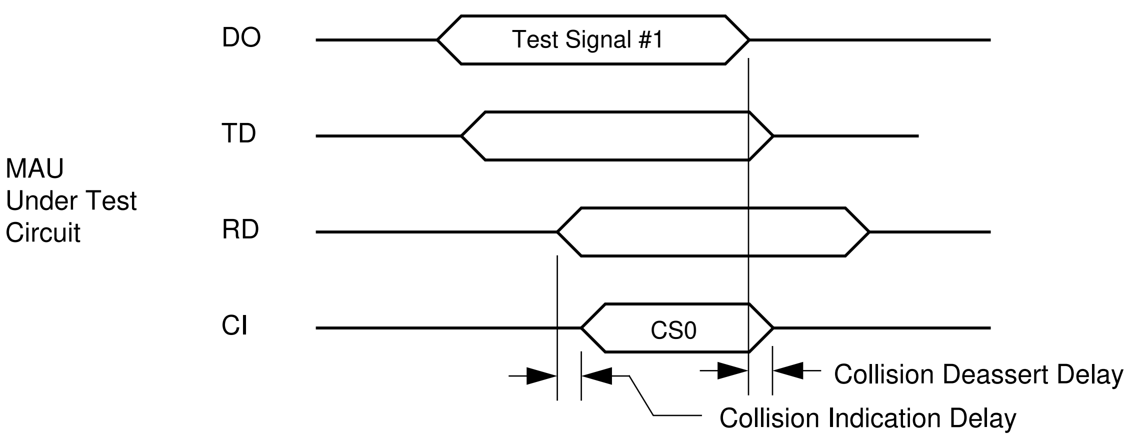
Conformance	:	While a collision is detected, a CS0 signal (see 7.3.1.2) shall be sent on the CI circuit.

Test Case ID	:	1411.04.03
Test Case Name	:	Collision indication delay.
Status	:	MANDATORY
Standard Reference	:	14.2.1.4
PICS Reference	:	14.10.4.5.5/2
History	:	
Test Purpose	:	To verify the delay between the collision start and the collision presence state indicated on CI circuit.
Note	:	
Test Setup	:	Test setup O.
Test Procedure	:	Monitor the CI circuit, DO circuit and RD circuit of the MAU under test. (1) Apply test signal 1 to the DO circuit of the tester MAU. Apply test signal 1 to the DO circuit of the MAU under test to create a collision. Measure the delay from collision start (application of the second test signal on the DO circuit of the MAU under test) to commencement of the CS0 signal on the CI circuit (see Fig 6-1a). (2) Apply test signal 1 to the DO circuit of the MAU under test. Apply test signal 1 to the DO circuit of the tester MAU to create a collision. Measure the delay from collision start (appearance of the second test signal on the RD circuit of the MAU under test) to commencement of the CS0 signal on the CI circuit (see Fig 6-1b).
Conformance	:	The CS0 signal shall be presented to the CI circuit no more than 9 bit times after the occurrence of a collision.

Test Case ID	:	1411.04.04
Test Case Name	:	Collision indication deassert delay.
Status	:	MANDATORY
Standard Reference	:	14.2.1.4
PICS Reference	:	14.10.4.5.5/3
History	:	
Test Purpose	:	To verify the cessation of the CS0 signal after the collision condition is removed.
Note	:	
Test Setup	:	Test setup O.
Test Procedure	:	Monitor the CI circuit, DO circuit and RD circuit of the MAU under test. (1) Apply test signal 1 to the DO circuit of the tester MAU. Apply test signal 1 to the DO circuit of the MAU under test to create a collision. Monitor the CI circuit for the presence of the CS0 signal. Stop the application of the test signal on the DO circuit of the tester MAU. Measure the time from the last transition of the test signal on the RD circuit of the MAU under test until the CS0 signal on the CI circuit stops (see Fig 6-1a). (2) Apply test signal 1 to the DO circuit of the MAU under



a) Test Signal Applied to Tester MAU Then MAU Under Test



b) Test Signal Applied to -MAU Under Test Then Tester MAU

Fig 6-1
Test Signal Application Timing for Collision Functions

		test. Apply test signal 1 to the DO circuit of the tester MAU to create a collision. Monitor the CI circuit for the presence of the CS0 signal. Stop the application of the test signal on the DO circuit of the MAU under test. Measure the time from the last transition of the test signal on the DO circuit of the MAU under test until the CS0 signal on the CI circuit stops (see Fig 6-1b).
Conformance	:	The CS0 signal on the CI circuit shall be deasserted within 9 bit times after the DO circuit or the RD circuit changes from active to idle.

Test Case ID	:	1411.04.05
Test Case Name	:	DI circuit source switch delay from CS0 assert.
Status	:	MANDATORY
Standard Reference	:	14.2.1.4
PICS Reference	:	14.10.4.5.5/5
History	:	
Test Purpose	:	To verify the delay between the start of collision and the presence of RD data on the DI circuit.
Note	:	
Test Setup	:	Test setup M.
Test Procedure	:	Apply test signal 19a to the DO circuit of the MAU under test. Monitor the CI circuit and DI circuit of the MAU under test. Apply test signal 19b to the DO circuit of the tester MAU at least 65 BT after the test signal on the MAU under test is applied to create a collision. Monitor the CI circuit for the presence of the CS0 signal. Measure the delay between the assertion of CS0 and commencement of *input* on the DI circuit corresponding to the test signal applied to the tester MAU. The signals applied to the DO circuit of the tester MAU and the DO circuit of the MAU under test are different to facilitate differentiation between DO loopback and RD.
Conformance	:	When CS0 is asserted on the CI circuit due to a collision, the data on the RD circuit shall be sent to the DI circuit within 9 bit times.

Test Case ID	:	1411.04.06
Test Case Name	:	DI circuit source switch delay from CS0 deassert.
Status	:	MANDATORY
Standard Reference	:	14.2.1.4
PICS Reference	:	14.10.4.5.5/6
History	:	
Test Purpose	:	To verify the delay between the end of collision and the presence of DO data on the DI circuit.
Note	:	
Test Setup	:	Test setup M.
Test Procedure	:	Apply the test signal 19a to the DO circuit of the MAU under test. Monitor the CI circuit, RD circuit and DI circuit of the MAU under test. Apply test signal 19b to the DO circuit of the tester MAU at least 65 BT after the test signal on the MAU under test is applied to create a collision. Monitor the CI circuit for the presence of the CS0 signal. After CS0 is asserted stop

		transmitting on the DO circuit of the tester MAU. Measure the delay between idle on the RD circuit [14.2.2.5] and the presence of the DO circuit test signal on the DI circuit. The signals applied to the DO circuit of the tester MAU and the DO circuit of the MAU under test should be different to facilitate differentiation between RD circuit data and DO loopback.
Conformance	:	When the RD circuit changes from active to idle and data is present on the DO circuit, the data on the DO circuit shall be sent to the DI circuit within 9 bit times.

6.2.1.5 Test Group 1411.05 - SQE Test Functions

Test Group ID	:	1411.05
Test Group Name	:	*Signal_quality_error* Message (SQE) Test Functions.
Test Group Purpose	:	To verify the functional characteristics of the SQE Test function.

Test Case ID	:	1411.05.01
Test Case Name	:	SQE_test_timer range.
Status	:	CONDITIONAL (SQE Test function shall be performed by MAUs connected to DTEs and shall not be performed for MAUs connected to repeaters).
Standard Reference	:	14.2.1.5
PICS Reference	:	14.10.4.5.6/3, 14.10.4.5.6/4
History	:	
Test Purpose	:	To verify the duration of the SQE Test state after the end of a frame transmission.
Note	:	Duration of CS0 is between first excursion outside 0 ±40 mV and the last positive transition.
Test Setup	:	Test setup B.
Test Procedure	:	Apply test signal 1 to the DO circuit of the MAU. Monitor the CI circuit. Measure duration of the CS0 signal on the CI circuit.
Conformance	:	The MAU shall send CS0 on the CI circuit for a time ‘SQE_test’ beginning a time ‘SQE_test_wait’ after the last positive transition on the DO circuit. The value of ‘SQE_test’ shall be 10 ± 5 bit times.

Test Case ID	:	1411.05.02
Test Case Name	:	SQE_test_wait_timer range.
Status	:	CONDITIONAL (SQE Test function shall be performed by MAUs connected to DTEs and shall not be performed for MAUs connected to repeaters).
Standard Reference	:	14.2.1.5
PICS Reference	:	14.10.4.5.6/2
History	:	
Test Purpose	:	To verify the duration of the SQE Test Wait state after the end of a frame transmission.
Note	:	Duration of CS0 is between first excursion outside 0 ±40 mV and the last positive transition.
Test Setup	:	Test setup B.
Test Procedure	:	Apply test signal 1 to the DO circuit of the MAU. Monitor the DO circuit and CI circuit. Measure time delay between the last

		positive transition of the data on the DO circuit and the assertion of CS0 on the CI circuit.
Conformance	:	The MAU shall send CS0 on the CI circuit beginning a time 'SQE_test_wait' after the last positive transition of a packet on the DO circuit. The value of 'SQE_test_wait' shall be between 0.6 µs and 1.6 µs.

Test Case ID	:	1411.05.03
Test Case Name	:	SQE Test function interference.
Status	:	CONDITIONAL (SQE Test function shall be performed by MAUs connected to DTEs and shall not be performed for MAUs connected to repeaters).
Standard Reference	:	14.2.1.5
PICS Reference	:	14.10.4.5.6/1
History	:	
Test Purpose	:	To verify the effect of the SQE Test function on the TD and DI circuits.
Note	:	Extraneous signal on the TD circuit is defined to be greater than ±50 mV; extraneous signal on the DI circuit is defined to be greater than ±40 mV.
Test Setup	:	Test setup B.
Test Procedure	:	Apply test signal 1 to the DO circuit of the MAU. Monitor the DI circuit and TD circuit for 3 µs after the end of frame transmission.
Conformance	:	This function should not introduce extraneous signals on the TD circuit or the DI circuit.

Test Case ID	:	1411.05.04
Test Case Name	:	SQE Test function in link fail state.
Status	:	CONDITIONAL (SQE Test function shall be performed by MAUs connected to DTEs and shall not be performed for MAUs connected to repeaters).
Standard Reference	:	14.2.1.5
PICS Reference	:	14.10.4.5.6/5
History	:	
Test Purpose	:	To verify that the SQE Test function does not transmit a CS0 signal when MAU is in a Link Test Fail state.
Note	:	
Test Setup	:	Test setup N.
Test Procedure	:	Apply power to the MAU under test. Monitor the AUI CI circuit of the MAU under test. Wait for 151 ms then apply test signal 1 to the DO circuit of the MAU under test. Check that the MAU is in a Link Test Fail state. Verify that CS0 is not asserted on the CI circuit for at least 3.1 µs.
Conformance	:	The CS0 signal shall not be sent by the SQE Test function while in any of the Link Test Fail states.

6.2.1.6 Test Group 1411.06 - Jabber Functions

Test Group ID	:	1411.06
Test Group Name	:	Jabber Functions.
Test Group Purpose	:	To verify the functional characteristics of the Jabber Test func-

tion.

Test Case ID	:	1411.06.01
Test Case Name	:	Xmit_max_timer range.
Status	:	MANDATORY
Standard Reference	:	14.2.1.6
PICS Reference	:	14.10.4.5.7/2, 14.10.4.5.7/3
History	:	
Test Purpose	:	To verify that jabber transmission inhibit starts within the time required.
Note	:	
Test Setup	:	Test setup C.
Test Procedure	:	Apply test signal 3a to the DO circuit of the MAU. Monitor the DI circuit, TD circuit and CI circuit. Check that the TD circuit and DI circuit signals are present up to 20 ms following the application of the input signal and that they are absent after 150 ms following the application of the input. Check that CS0 is asserted on the CI circuit after the 150 ms time period. Repeat the same procedure using test signal 3b.
Conformance	:	The MAU shall provide a window 'xmit_max' during which time the Transmit function may continuously transmit *TD_output* messages to the TD circuit. The value of 'xmit_max' shall be between 20 ms and 150 ms. If a transmission exceeds this duration the Jabber function shall inhibit the Loopback function and the transmission of *TD_output* messages by the Transmit function and shall send the CS0 signal on the CI circuit.

Test Case ID	:	1411.06.02
Test Case Name	:	Jabber reset.
Status	:	MANDATORY
Standard Reference	:	14.2.1.6
PICS Reference	:	14.10.4.5.7/1, 14.10.4.5.7/4
History	:	
Test Purpose	:	To verify the jabber function reset mechanism.
Note	:	
Test Setup	:	Test setup C.
Test Procedure	:	Apply test signal 3a to the DO circuit of the MAU. Monitor the DI circuit, TD circuit and CI circuit. When jabber is indicated (signals no longer present on the DI and TD circuits and CS0 is asserted on the CI circuit), stop the test signal. Wait 249 ms from when the test signal is stopped and verify that CS0 is still present on the CI circuit and that no signals are present on the TD circuit and DI circuit. Wait an additional 502 ms and verify that CS0 is no longer asserted on the CI circuit. Repeat the above procedure using test signal 3b.
Conformance	:	If a transmission exceeds 'xmit_max' the Jabber function shall inhibit the Loopback function and the transmission of *TD_output* messages by the Transmit function and shall send the CS0 signal on the CI circuit. This shall continue until *output_idle* has been continuously present on the DO circuit for a time 'unjab'. The value of 'unjab' shall be 0.5 $\pm$ 0.25 s.

Test Case ID	:	1411.06.03
Test Case Name	:	Jabber lockup protection.
Status	:	MANDATORY
Standard Reference	:	14.2.1.6
PICS Reference	:	14.10.4.5.7/5
History	:	
Test Purpose	:	To verify the MAU jabber lockup protection.
Note	:	
Test Setup	:	Test setup B.
Test Procedure	:	Apply test signal 26 to the DO circuit of the MAU. Monitor the TD circuit. Verify that the MAU does not enter jabber by verifying that the TD circuit remains active.
Conformance	:	The MAU shall not activate its Jabber function when the repeater's MAU Jabber Lockup Protection function operates at its longest permitted time as specified in 9.6.5.

6.2.1.7 Test Group 1411.07 - Link Integrity Test Functions

Test Group ID	:	1411.07
Test Group Name	:	Link Integrity Test Functions.
Test Group Purpose	:	To verify the functional characteristics of the Link Test functions.

Test Case ID	:	1411.07.01
Test Case Name	:	Link loss timer.
Status	:	MANDATORY
Standard Reference	:	14.2.1.7
PICS Reference	:	14.10.4.5.8/1
History	:	
Test Purpose	:	To verify the value of the 'link_loss' timer.
Note	:	
Test Setup	:	Test setup B.
Test Procedure	:	Apply test signal 4 to the DO circuit of the MAU. Monitor the DI circuit and TD circuit. Stop applying the link test pulses to the RD circuit. Measure the time from the last link test pulse to the loss of loopback on the DI circuit.
Conformance	:	If neither *RD_input* nor a link test pulse is received for a time 'link_loss', the MAU shall enter the Link Test Fail state and cause the *input_idle* message to be sent on the DI circuit and the *TD_idle* message to be sent on the TD circuit (Fig 14-6). The value of 'link_loss' shall be between 50 and 150 ms.

Test Case ID	:	1411.07.02
Test Case Name	:	Acceptance range for consecutive link test pulses.
Status	:	MANDATORY
Standard Reference	:	14.2.1.7
PICS Reference	:	14.10.4.5.8/6, 14.10.4.5.8/7
History	:	
Test Purpose	:	To verify acceptance range for consecutive link test pulses.
Note	:	

Test Setup : Test setup B.
Test Procedure : Apply power to the MAU. Stop applying the link test pulses to the RD circuit. Check that the MAU is in a Link Test Fail state. Monitor the DO circuit and DI circuit. Apply a test signal consisting of 11 link test pulses that are spaced 7.1 ms apart to the RD circuit of the MAU. Apply test signal 1 to the DO circuit of the MAU. Verify loopback presence on the DI circuit. Repeat the test procedure with 24 ms spacing between link test pulses.
Conformance : Only link test pulses that occur within time 'link_test_max' of each other shall be considered consecutive. The value of 'link_test_max' shall be between 25 and 150 ms. In addition, detected pulses that occur within a time 'link_test_min' of a previous pulse or packet shall be ignored while in the Link Test Pass state. In the Link Test Fail state, such pulses shall reset the counted number of consecutive link test pulses to zero. The value of 'link_test_min' shall be between 2 and 7 ms.

Test Case ID : 1411.07.03
Test Case Name : Link test pulses outside acceptance range (while in Link Test Pass state).
Status : MANDATORY
Standard Reference : 14.2.1.7
PICS Reference : 14.10.4.5.8/8
History :
Test Purpose : To verify the rejection range for consecutive link test pulses while the MAU is in the Link Test Pass state.
Note : *This test case is considered untestable. It is not practical to measure and is not considered critical. Even though testing for compliance is not practical, conformance to the standard, **by design**, is the responsibility of the manufacturer with compliance status to be noted in the PICS.*
Test Setup :
Test Procedure :
Conformance : Detected pulses that occur within a time 'link_test_min' of a previous pulse or packet shall be ignored while in the Link Test Pass state. The value of 'link_test_min' shall be between 2 and 7 ms.

Test Case ID : 1411.07.04
Test Case Name : Link test pulses outside acceptance range (not in the Link Test Pass state).
Status : MANDATORY
Standard Reference : 14.2.1.7
PICS Reference : 14.10.4.5.8/9
History :
Test Purpose : To verify the rejection range for consecutive link test pulses while the MAU is not in Link Test Pass state.
Note :
Test Setup : Test setup B.
Test Procedure : Apply power to the MAU. Stop applying link test pulses to the RD circuit. Check that the MAU is in a Link Test Fail state. Monitor the DO circuit and DI circuit. Apply a test signal con-

		sisting of 11 link test pulses that are spaced 1.9 ms apart to the RD circuit of the MAU. Check that the MAU is still in a Link Test Fail state. Apply test signal 1 to the DO circuit of the MAU. Verify that loopback is disabled. Repeat the test procedure with 151 ms spacing between link test pulses.
Conformance	:	Only link test pulses that occur within time 'link_test_max' of each other shall be considered consecutive. The value of 'link_-test_max' shall be between 25 and 150 ms. In addition, detected pulses that occur within a time 'link_test_min' of a previous pulse or packet shall be ignored while in the Link Test Pass state. In the Link Test Fail state, such pulses shall reset the counted number of consecutive link test pulses to zero. The value of 'link_test_min' shall be between 2 and 7 ms.

Test Case ID	:	1411.07.05
Test Case Name	:	Link fail effect on MAU functions.
Status	:	MANDATORY
Standard Reference		14.2.1.7
PICS Reference	:	14.10.4.5.8/2-4, 14.10.4.5.8/10-14
History	:	
Test Purpose	:	To verify that the following MAU functions are disabled, while the MAU is not in the Link Pass state: Transmit, Receive, Loopback, Collision Presence and SQE test.
Note	:	Some of these tests will cause a transition to the Link Test Pass state after the test signal ends. Before continuing the tests, make sure that the MAU under test returns to a Link Test Fail state.
Test Setup	:	Test setup N.
Test Procedure	:	Apply power to the MAU. For each of the following scenarios check that the MAU is in a Link Test Fail state before applying the test signal(s) to the specified circuit(s): (1) **Transmit.** Apply test signal 1 to the DO circuit of the MAU under test while monitoring the TD circuit for TP_IDL. (2) **Receive.** Apply test signal 1 to the DO circuit of the tester MAU while monitoring the DI circuit of the MAU under test for IDL. (3) **Loopback.** Apply test signal 1 to the DO circuit of the MAU under test while monitoring the DI circuit of the MAU under test for IDL. (4) **Collision Presence.** Apply test signal 1 to the DO circuit of the tester MAU and test signal 1 to the DO circuit of the MAU under test to create a collision. Monitor the CI circuit of the MAU under test for IDL. (5) **SQE Test.** Apply test signal 1 to the DO circuit of the MAU under test. Monitor the CI circuit for no SQE.
Conformance	:	While the MAU is not in the Link Test Pass state the Link Integrity Test function shall disable the bit transfer of the Transmit, Receive and Loopback functions, and the Collision Presence and SQE Test functions.

Test Case ID	:	1411.07.06

Test Case Name	:	Link Test Fail Extend state exit.
Status	:	MANDATORY
Standard Reference	:	14.2.1.7
PICS Reference	:	14.10.4.5.8/15
History	:	
Test Purpose	:	To verify that the MAU functions are re-enabled only after the RD and DO circuits become idle.
Note	:	
Test Setup	:	Test setup N.
Test Procedure	:	Apply power to the MAU under test. Check that the MAU under test is in a Link Test Fail state. Apply test signal 5 to the DO circuit of the MAU under test. After 1 ms, apply test signal 1 to the DO circuit of the tester MAU. Verify that DI loopback occurs on the second packet from the DO circuit of the MAU under test, but not on the first packet.
Conformance	:	Re-enabling shall be deferred until the signals on the RD and DO circuits become idle.

6.2.1.8 Test Group 1411.08 - MAU State Machines

Test Group ID	:	1411.08
Test Group Name	:	MAU State Machines.
Test Group Purpose	:	To verify proper operation of the MAU state machines.

Test Case ID	:	1411.08.01
Test Case Name	:	MAU transmit, receive, loopback and collision state diagram.
Status	:	MANDATORY
Standard Reference	:	Fig 14-3
PICS Reference	:	14.10.4.5.9/1
History	:	
Test Purpose	:	To verify the MAU transmit, receive, loopback and collision presence functions.
Note	:	Test case coverage for this test is shown in Fig A1.
Test Setup	:	Use the following test setups for each subtest below. (1) As specified in each individual test case. (2) Test setup N. (3) Test setup P. (4) Test setup O. (5) Test setup O. (6) Test setup B.
Test Procedure	:	Apply power to the MAU. (1) Perform the following tests, using the procedure(s) as specified in each test case: 1411.01.04, 1411.02.02, 1411.03.01, 1411.04.01, 1411.04.02, 1411.04.04 and 1411.04.05. (2) Check that the MAU under test is in a Link Test Fail state. Monitor the DI circuit of the MAU under test. Apply test signal 1 to the DO circuit of the tester MAU. Verify that the test signal does not appear on the DI circuit of the MAU under test. (3) Apply test signal 3a to the DO circuit of the MAU under test. Monitor the DI circuit, RD circuit and CI circuit of the MAU under test. When jabber is indicated (CS0 is

asserted on the CI circuit), apply test signal 1 to the DO circuit of the tester MAU. Verify that the RD test signal appears on the DI circuit of the MAU under test.

(4) Monitor the DI circuit, DO circuit and RD circuit of the MAU under test. Apply test signal 6 to the DO circuit of the tester MAU. Apply test signal 1 to the DO circuit of the MAU under test such that the start and end of frame occurs while test signal 6 is active (see Fig 6-2a). Verify that DI is active for the duration of test signal 6 on the RD circuit.

(5) Monitor the DI circuit, DO circuit and RD circuit of the MAU under test. Apply test signal 6 to the DO circuit of the MAU under test. Apply test signal 1 to the DO circuit of the tester MAU such that the start and end of frame occurs while test signal 6 is active (see Fig 6-2b). Verify that DI is active for the duration of test signal 6 on the DO circuit.

(6) Apply IDL to the DO circuit of the MAU. Monitor the CI circuit, DI circuit and TD circuit. Verify that the CI circuit and DI circuit are asserting IDL and the TD circuit is asserting TP_IDL.

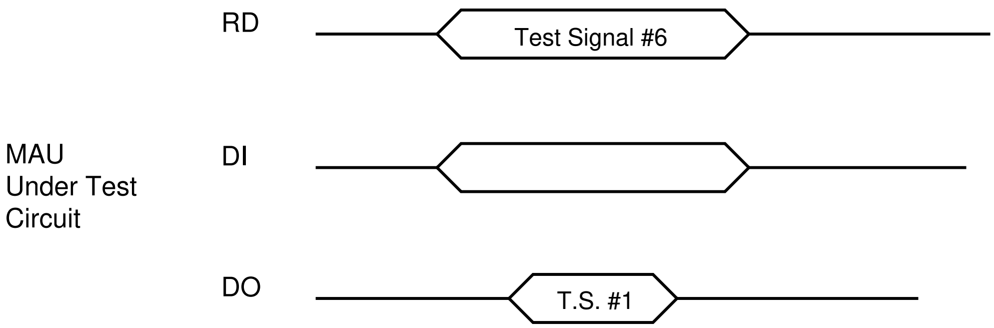
Conformance : Meets the requirements of Fig 14-3.

Test Case ID : 1411.08.02
Test Case Name : *Signal_quality_error* message test function state diagram.
Status : CONDITIONAL (SQE Test function shall be performed by MAUs connected to DTEs and shall not be performed for MAUs connected to repeaters).
Standard Reference : Fig 14-4
PICS Reference : 14.10.4.5.9/2
History :
Test Purpose : To verify the *signal_quality_error* message test function.
Note : Test case coverage for this test is shown in Fig A2.
Test Setup : Use the test setups as specified in each individual test case.
Test Procedure : Perform the following tests, using the procedure(s) as specified in each test case: 1411.05.01, 1411.05.02 and 1411.05.04.
Conformance: : Meets the requirements of Fig 14-4.

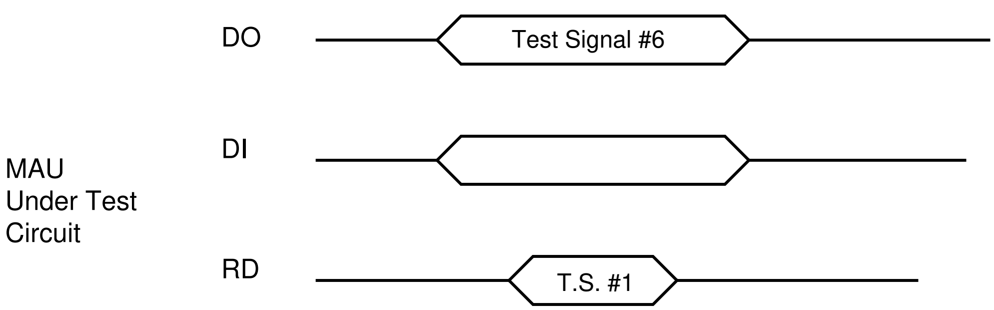
Test Case ID : 1411.08.03
Test Case Name : Jabber function state diagram.
Status : MANDATORY
Standard Reference : Fig 14-5
PICS Reference : 14.10.4.5.9/3
History :
Test Purpose : To verify the jabber function state diagram.
Note : Test case coverage for this test is shown in Fig A3.
Test Setup : Test setup C.
Test Procedure : Disable the LTPG, apply power to the MAU and check that the MAU is in a Link Test Fail state.

(1) Perform the following tests, using the procedure(s) as specified in each test case: 1411.06.01 and 1411.06.02.

(2) Monitor the DI circuit, TD circuit and CI circuit of the



a) Test Signal Applied to Tester MAU Then MAU Under Test



b) Test Signal Applied to MAU Under Test Then Tester MAU

Fig 6-2
Test Signal Application Timing for Collision State Diagram

MAU. Apply test signal 3a to the DO circuit of the MAU for at least 151 ms. When jabber is indicated (SQE is asserted on the CI circuit), stop the test signal. Wait for 249 ms, verify that SQE is still asserted on the CI circuit, then reapply the test signal for a duration of 512 bit times. Stop the test signal, wait for another 249 ms then reapply the test signal for a duration of 512 bit times. Stop the test signal, wait for another 249 ms then reapply the test signal for a duration of 512 bit times. Stop the test signal, wait for another 249 ms then reapply the test signal for a duration of 512 bit times. Verify that SQE is still asserted on the CI circuit. Wait 502 ms, then reapply the test signal. Verify that the CI circuit is idle.

(3) Monitor the DI circuit, TD circuit and CI circuit of the MAU. Apply test signal 5 to the DO circuit of the MAU. Verify that the TD signals and DI signals follow DO and that CS0 is not asserted on the CI circuit.

Enable the LTPG, check that the MAU is in the Link Test Pass state and repeat tests (1) and (2) above.

Conformance : Meets the requirements of Fig 14-5.

Test Case ID : 1411.08.04
Test Case Name : Link integrity test function state diagram.
Status : MANDATORY
Standard Reference : Fig 14-6
PICS Reference : 14.10.4.5.9/4
History :
Test Purpose : To verify the link integrity test function state diagram.
Note : Test case coverage for this test is shown in Fig A4.
Test Setup : Use the following test setups for each subtest below.

(1) As specified in each individual test case.
(2) Test setup N.
(3) Test setup B
(4) Test setup M

Test Procedure : Perform each subtest listed below.

(1) Perform the following tests, using the procedure(s) specified in each test case: 1411.01.04, 1411.02.02, 1411.03.01, 1411.07.01 through 1411.07.06 inclusive.

(2) Monitor the DI circuit and TD circuit of the MAU under test. Apply power to the MAU and check that the MAU is in a Link Test Fail state. Apply test signal 1 to the DO circuit of the tester MAU and verify the presence of IDL on the DI circuit of the MAU under test. Apply test signal 1 to the DO circuit of the MAU under test within 1 ms and verify that the test signal appears on the TD circuit of the MAU under test.

(3) Monitor the DI circuit. Apply power to the MAU and check that the MAU is in the Link Test Pass state. Apply test signal 2a to the DO circuit of the MAU under test. Stop the transmission of link test pulses onto the RD circuit. After the MAU has entered a Link Test Fail state as indicated by the cessation of DI activity, wait

7.1 ms then send one link test pulse. Apply test signal 1 to the DO circuit of the MAU within 1-2 ms of the link test pulse. Verify that no loopback signals appear on the DI circuit.

(4) Monitor the DI circuit of the MAU under test. Apply power to the MAU and check that the MAU is in the Link Test Pass state. Apply test signal 18 to the DO circuit of the tester MAU. Apply test signal 1 to the DO circuit of the MAU under test within 1 ms of the end of the last packet on the RD circuit. Verify that the test signal appears on the DI circuit.

Conformance : Meets the requirements of Fig 14-6.

6.2.1.9 Test Group 1411.09 - Isolation Requirements

Test Group ID : 1411.09
Test Group Name : Isolation Requirements.
Test Group Purpose : To verify proper isolation on the MDI leads.

Test Case ID : 1411.09.01
Test Case Name : Isolation, MDI leads to DTE Physical Layer circuits.
Status : MANDATORY
Standard Reference : 14.3.1.1
PICS Reference : 14.10.4.5.11/1
History :
Test Purpose : To verify the electrical isolation between the MDI leads and the DTE Physical Layer circuits, including frame ground.
Note : Test case 1411.09.02 must be run after this test is completed.
Test Setup : Test setup CC.
Test Procedure : Apply one of the following voltages as E_{iso} between each pin of the AUI connector (including PG, the AUI shell) and each pin of the MDI connector. For embedded MAUs, apply E_{iso} between Frame Ground of the MAU (as specified in the PIXIT) and each pin of the MDI connector.

(1) 1500 V rms at 50 to 60 Hz for 60 s, applied as specified in Section 5.3.2 of IEC Publication 950 [9].
(2) 2250 Vdc for 60 s, applied as specified in Section 5.3.2 of IEC Publication 950 [9].
(3) A sequence of ten 2400 V impulses of alternating polarity, applied at intervals of not less than 1 s. The shape of the impulses shall be 1.2/50 μs, as defined in IEC Publication 60 [8].

Verify that there is no insulation breakdown during the test.

Conformance : The MAU shall provide isolation between the DTE Physical Layer circuits including frame ground and all MDI leads including those not used by 10BASE-T. This electrical separation shall withstand at least one of the following electrical strength tests.

(1) 1500 V rms at 50 to 60 Hz for 60 s, applied as specified in Section 5.3.2 of IEC Publication 950 [9].
(2) 2250 Vdc for 60 s, applied as specified in Section 5.3.2 of IEC Publication 950 [9].
(3) A sequence of ten 2400 V impulses of alternating polar-

ity, applied at intervals of not less than 1 s. The shape of the impulses shall be 1.2/50 µs (1.2 µs virtual front time, 50 µs virtual time of half value), as defined in IEC Publication 60 [8].

There shall be no insulation breakdown, as defined in Section 5.3.2 of IEC Publication 950 [9], during the test.

Test Case ID	:	1411.09.02
Test Case Name	:	Resistance after breakdown test.
Status	:	MANDATORY
Standard Reference	:	14.3.1.1
PICS Reference	:	14.10.4.5.11/2
History	:	
Test Purpose	:	To verify the resistance between the MDI leads and the DTE Physical Layer circuits, including frame ground.
Note	:	Test case 1411.09.01 must be run prior to this test.
Test Setup	:	Test Setup DD.
Test Procedure	:	Apply 500 Vdc between each pin of the AUI connector (including PG, the AUI shell) and each pin of the MDI connector. For embedded MAUs, apply 500 Vdc between Frame Ground of the MAU (as specified in the PIXIT) and each pin of the MDI connector. Verify that the dc current is less than 250 µA.
Conformance	:	The resistance after the test shall be at least 2 MΩ, measured at 500 Vdc.

6.2.1.10 Test Group 1411.10 - Transmitter Specification

Test Group ID	:	1411.10
Test Group Name	:	Transmitter Specification.
Test Group Purpose	:	To verify transmitted signal parameters.

Test Case ID	:	1411.10.01
Test Case Name	:	TD circuit short circuit current.
Status	:	MANDATORY
Standard Reference	:	14.3.1.2.7
PICS Reference	:	14.10.4.5.12/12, 14.10.4.5.12/13
History	:	
Test Purpose	:	To verify the transmitter fault tolerance.
Note	:	
Test Setup	:	Test setup R.
Test Procedure	:	Apply power to the MAU. Monitor the peak output current of the TD circuit of the MAU while applying a short circuit across the TD circuit for 10 seconds. Apply test signal 4 to the DO circuit of the MAU. Continue monitoring the output current of the TD circuit for an additional 10 seconds. Remove the short circuit. Verify that when the fault condition is removed the circuit operates normally by performing the remainder of the transmitter tests (group ID 1411.10).
Conformance	:	Transmitters, when either idle or non-idle, shall withstand without damage the application of short circuits across the TD circuit for an indefinite period of time and shall resume normal operation after such faults are removed. The magnitude of the

current through such a short circuit shall not exceed 300 mA.

Test Case ID	:	1411.10.02
Test Case Name	:	Peak differential output voltage on TD circuit.
Status	:	MANDATORY
Standard Reference	:	14.3.1.2.1
PICS Reference	:	14.10.4.5.12/1
History	:	
Test Purpose	:	To verify the TD circuit peak differential output voltage.
Note	:	
Test Setup	:	Test setup B.
Test Procedure	:	Apply test signal 1 to the DO circuit of the MAU. Monitor the peak differential voltage on the TD circuit across the 100 Ω load.
Conformance	:	The peak differential voltage on the TD circuit when terminated with a 100 Ω resistive load shall be between 2.2 V peak and 2.8 V peak for all data sequences.

Test Case ID	:	1411.10.03
Test Case Name	:	Harmonic content, all ones signal.
Status	:	MANDATORY
Standard Reference	:	14.3.1.2.1
PICS Reference	:	14.10.4.5.12/2
History	:	
Test Purpose	:	To verify the harmonic content at the output of transmitter.
Note	:	
Test Setup	:	Test setup T.
Test Procedure	:	Apply test signal 5 to the DO circuit of the MAU. Monitor the harmonic content of the TD circuit signal using the spectrum analyzer.
Conformance	:	When the DO circuit is driven by an all ones Manchester signal each harmonic measured at the output of the transmitter shall be at least 27 dB below the fundamental.

Test Case ID	:	1411.10.04
Test Case Name	:	Output waveform, with scaling of voltage template.
Status	:	MANDATORY
Standard Reference	:	14.3.1.2.1
PICS Reference	:	14.10.4.5.12/3
History	:	
Test Purpose	:	To verify the transmitter output equalization.
Note	:	See Section 14, Appendix A4.3.1, for measurement details.
Test Setup	:	Test setup A.
Test Procedure	:	Apply test signal 1 to the DO circuit of the MAU. Monitor the TD circuit signal. An oscilloscope set for a zero voltage trigger with a positive slope is allowed to accumulate an eye pattern that must be within the template. Acquisition must be long enough to ensure that all data variations have been observed. When using packetized data, the TP_IDL and the first transmitted bit should be excluded from this measurement. Repeat-

		ed applications of the test signal may be necessary to acquire enough data to build a definite eye pattern.
Conformance	:	The TD transmitter shall provide equalization such that the output waveform shall fall within the template shown in Fig 14-9 for all data sequences. Voltage and time coordinates for inflection points on Fig 14-9 are given in Table 14-1. (Zero crossing points are different for external and internal MAUs. The zero crossings depicted in Fig 14-9 apply to an external MAU.) The template voltage may be scaled by a factor of 0.9 to 1.1 but any scaling below 0.9 or above 1.1 shall not be allowed. The recommended measurement procedure is described in A4.3.1. Time t = 0 on the template represents a zero crossing, with positive slope, of the output waveform.

Test Case ID	:	1411.10.05
Test Case Name	:	Output waveform with scaling of voltage template (inverted template).
Status	:	MANDATORY
Standard Reference	:	14.3.1.2.1
PICS Reference	:	14.10.4.5.12/3
History	:	
Test Purpose	:	To verify the transmitter output equalization.
Note	:	
Test Setup	:	Test setup A.
Test Procedure	:	Apply test signal 1 to the DO circuit of the MAU. Monitor the TD circuit signal. An oscilloscope set for a zero voltage trigger with a negative slope is allowed to accumulate an eye pattern that must be within the template. Acquisition must be long enough to ensure that all data variations have been observed. When using packetized data, the TP_IDL and the first transmitted bit should be excluded from this measurement. Repeated applications of the test signal may be necessary to acquire enough data to build a definite eye pattern.
Conformance	:	The TD transmitter shall provide equalization such that the output waveform shall fall within the template shown in Fig 14-9 for all data sequences. Voltage and time coordinates for inflection points on Fig 14-9 are given in Table 14-1. (Zero crossing points are different for external and internal MAUs. The zero crossings depicted in Fig 14-9 apply to an external MAU.) The template voltage may be scaled by a factor of 0.9 to 1.1 but any scaling below 0.9 or above 1.1 shall not be allowed. The recommended measurement procedure is described in A4.3.1. Time t = 0 on the template represents a zero crossing, with negative slope, of the output waveform.

Test Case ID	:	1411.10.06
Test Case Name	:	Start of TP_IDL waveform, with specified loads, with and without the cable model.
Status	:	MANDATORY
Standard Reference		14.3.1.2.1
PICS Reference	:	14.10.4.5.12/4
History	:	

Test Purpose	:	To verify the characteristics of the transmitter output after transition to idle state.
Note	:	
Test Setup	:	Test setup D.
Test Procedure	:	Apply test signal 1 to the DO circuit of the MAU. Monitor the TD circuit signal at the test load for each of the test loads shown in Fig 14-11. Repeat the test without the TPM in the Test Setup and the test loads connected directly to the TD circuit.
Conformance	:	The TP_IDL shall always start with a positive waveform when a waveform conforming to Fig. 7-12 is applied to the DO circuit. If the last bit transmitted was a CD1, the last transition will be at the bit cell center of the CD1. If the last bit transmitted was a CD0, the PLS will generate an additional transition at the bit cell boundary following the CD0. After the zero crossing of the last transition, the differential voltage shall remain within the shaded area of Fig 14-10. Once the differential voltage has gone more negative than -50 mV, it shall not exceed +50 mV. The template requirements of Fig 14-10 shall be met, when measured across each of the test loads defined in Fig 14-11; both with the load connected directly to the TD circuit and with the load connected through the twisted pair model as defined in Figs 14-7 and 14-8.

Test Case ID	:	1411.10.07
Test Case Name	:	TD circuit differential output impedance.
Status	:	MANDATORY
Standard Reference	:	14.3.1.2.2
PICS Reference	:	14.10.4.5.12/6
History	:	
Test Purpose	:	To verify the transmitter differential output impedance.
Note	:	See Section 14, Appendix A4.3.2 for measurement details.
Test Setup	:	Test setup Q.
Test Procedure	:	Using the network analyzer, measure the return loss between 5.0 MHz and 10.0 MHz with 0.5 MHz steps, utilizing a reference resistance of 100 Ω. Calculate the return loss using a reference resistance of 85 Ω and 111 Ω.
Conformance	:	The differential output impedance as measured on the TD circuit shall be such that any reflection, due to differential signals incident upon the TD circuit from a simplex link segment having any impedance within the range specified in 14.4.2.2 shall be at least 15 dB below the incident, over the frequency range of 5.0 to 10 MHz. This return loss shall be maintained at all times when the MAU is in the power-on state, including when the TD circuit is sending TP_IDL.

Test Case ID	:	1411.10.08
Test Case Name	:	Common mode to differential mode conversion.
Status	:	MANDATORY
Standard Reference	:	14.3.1.2.4
PICS Reference	:	14.10.4.5.12/9
History	:	

Test Purpose	:	To verify the transmitter impedance balance over the frequency range of 1.0 to 21 MHz.
Note	:	The balance of the test equipment (such as the matching of the 147 Ω resistors) must exceed that required of the transmitter.
Test Setup	:	Test setup E.
Test Procedure	:	Apply power. Apply a 1 MHz sine-wave with a 15 V peak amplitude to represent the E_{cm} signal and monitor the differential voltage at the TD circuit, E_{dif}, ignoring the Link Test Pulses. In steps of 2 MHz, increase the frequency up to a maximum of 21 MHz. For each step calculate the common mode to differential mode impedance balance as $20 \log_{10} (E_{cm} / E_{dif})$.
Conformance	:	The common mode to differential mode impedance balance of the transmitter shall exceed $29 - 17 \log_{10} (f / 10)$ dB (where f is the frequency in MHz) over the frequency range 1.0 to 20 MHz.

Test Case ID	:	1411.10.09
Test Case Name	:	TD circuit common mode output voltage.
Status	:	MANDATORY
Standard Reference	:	14.3.1.2.5
PICS Reference	:	14.10.4.5.12/10
History	:	
Test Purpose	:	To verify the common mode output voltage of the transmitter.
Note	:	The balance of the test equipment (such as the matching of the 47.5 Ω resistors) must exceed that required of the transmitter.
Test Setup	:	Test setup F.
Test Procedure	:	Apply test signal 1 to the DO circuit of the MAU. Measure the common mode output voltage E_{cm}.
Conformance	:	The magnitude of the total common mode output voltage of the transmitter, E_{cm}, measured as shown in Fig 14-14, shall be less than 50 mV peak.

Test Case ID	:	1411.10.10
Test Case Name	:	Transmitter common mode rejection, 15 V peak 10.1 MHz sinusoid.
Status	:	MANDATORY
Standard Reference	:	14.3.1.2.6
PICS Reference	:	14.10.4.5.12/11
History	:	
Test Purpose	:	To verify the transmitter common mode rejection.
Note	:	
Test Setup	:	Test setup E.
Test Procedure	:	Apply test signal 1 to the DO circuit of the MAU.Monitor the differential voltage at the TD circuit, E_{dif}. Establish a baseline jitter value by measuring the edge jitter at the TD circuit with a 0 V E_{cm} input. Apply a 15 V peak amplitude 10.1 MHz sine wave to represent the E_{cm} signal and measure the edge jitter.
Conformance	:	The application of E_{cm} as shown in Fig 14-13 shall not change the differential voltage at the TD circuit, E_{dif}, by more than 100 mV for all data sequences. Additionally, the edge jitter added by the application of E_{cm} shall be no more than 1.0 ns. E_{cm} shall be a 15 V peak 10.1 MHz sine wave.

Test Case ID	:	1411.10.11
Test Case Name	:	Link test pulse waveform, with specified loads, with and without the cable model.
Status	:	MANDATORY
Standard Reference	:	14.3.1.2.1
PICS Reference	:	14.10.4.5.12/5
History	:	
Test Purpose	:	To verify the characteristics of the Link Test Pulse waveform.
Note	:	
Test Setup	:	Test setup G.
Test Procedure	:	Monitor the TD circuit signal at the test load for each of the test loads shown in Fig 14-11. Repeat the test without the TPM in the Test Setup and with the test loads connected directly to the TD circuit.
Conformance	:	The link test pulse shall be a single positive (TD+ lead positive with respect to TD- lead) pulse which falls within the shaded area of Fig. 14-12. Once the differential output voltage has become more negative than -50 mV, it shall remain less than +50 mV. The template requirements of Fig 14-12 shall be met, when measured across each of the test loads defined in Fig 14-11; both with the load connected directly to the TD circuit and with the load connected through the twisted pair model as defined in Fig. 14-7 and 14-8.

Test Case ID	:	1411.10.12
Test Case Name	:	Transmitter output timing jitter with cable model.
Status	:	MANDATORY
Standard Reference	:	14.3.1.2.3
PICS Reference	:	14.10.4.5.12/7
History	:	
Test Purpose	:	To verify the jitter added by the MAU.
Note	:	
Test Setup	:	Test setup A.
Test Procedure	:	Apply test signal 6 to the DO circuit of the MAU. Monitor the DO circuit and TD circuit. Using the oscilloscope, measure the jitter of the zero crossings on the TD circuit. Disregard the first bit transmitted on the TD circuit and Start Of Idle (SOI). Set the oscilloscope to trigger on the DO circuit signal zero crossing with positive slope. Observe the zero crossings 8 and 8.5 BT from the triggering zero crossing. An external MAU is compliant when all zero crossings fall within the time intervals 8.0 BT ± 7 ns and 8.5 BT ± 7 ns.
Conformance	:	The jitter added to the signal on the DO circuit as it propagates through the MAU and twisted pair model shall be no more than ± 3.5 ns.

Test Case ID	:	1411.10.13
Test Case Name	:	Transmitter output timing jitter without cable model.
Status	:	MANDATORY
Standard Reference	:	14.3.1.2.3
PICS Reference	:	14.10.4.5.12/8

History	:	
Test Purpose	:	To verify the jitter added by the MAU when directly driving a 100 Ω resistive load.
Note	:	
Test Setup	:	Test setup B.
Test Procedure	:	Apply test signal 6 to the DO circuit of the MAU. Monitor the DO circuit and TD circuit. Using the oscilloscope, measure the jitter of the zero crossings on the TD circuit. Disregard the first bit transmitted on the TD circuit and Start Of Idle (SOI). Set the oscilloscope to trigger on the DO circuit signal zero crossing with positive slope. Observe the zero crossings 8 and 8.5 BT from the triggering zero crossing. An external MAU is compliant when all zero crossings fall within the time intervals 8.0 BT ± 16 ns and 8.5 BT ± 16 ns.
Conformance	:	The MAU shall add no more than ± 8 ns of jitter to the signal received on the DO circuit, when the TD circuit is directly driving a 100 Ω resistive load.

Test Case ID	:	1411.10.14
Test Case Name	:	Transmitter fault tolerance, impulse.
Status	:	MANDATORY
Standard Reference	:	14.3.1.2.7
PICS Reference	:	14.10.4.5.12/14
History	:	
Test Purpose	:	To verify the transmitter fault tolerance when a high voltage impulse is applied to the transmitter when idle and non-idle.
Note	:	The impulse shape should be adjusted while applied to the test object as per IEC Publication 60 [8].
Test Setup	:	Test setup AA.
Test Procedure	:	Apply a IEC standard full impulse voltage of positive polarity, with a peak value of 1000 V, a virtual front time of 300 ns and virtual time to half value of 50 µs as E_{cm} to the test setup. Repeat the test using a negative polarity impulse. Apply test signal 5 to the DO circuit of the MAU. Repeat the previous test procedure (both polarities). Verify that the transmitter still operates normally by performing the transmitter test group tests (group ID 1411.10).
Conformance	:	Transmitters, when either idle or non-idle, shall withstand without damage a 1000 V common-mode impulse applied at E_{cm} of either polarity (as indicated in Fig 14-15). The shape of the impulse shall be 0.3/50 µs (300 ns virtual front time, 50 µs virtual time of half value), as defined in IEC Publication 60 [8].

Test Case ID	:	1411.10.15
Test Case Name	:	Power cycle effect on TD circuit.
Status	:	MANDATORY
Standard Reference	:	14.3.2.3
PICS Reference	:	14.10.4.5.12/15
History	:	
Test Purpose	:	To verify proper operation of the TD circuit with power cycling.
Note	:	Extraneous signal on the TD circuit is defined to be greater than ±50 mV.

Test Setup : Test setup A.
Test Procedure : Monitor the TD circuit of the MAU. Turn the power to MAU off then on several times. Verify that no extraneous signals appear on the TD circuit.
Conformance : The MAU shall not introduce extraneous signals on the TD... circuits during normal power-up and power-down.

6.2.1.1 1 Test Group 141 1.11 - Receiver Specification

Test Group ID : 1411.11
Test Group Name : Receiver Specification.
Test Group Purpose : To ensure correct input signal handling of the receiver.

Test Case ID : 1411.11.01
Test Case Name : RD circuit fault tolerance, short circuit.
Status : MANDATORY
Standard Reference : 14.3.1.3.6
PICS Reference : 14.10.4.5.13/11
History :
Test Purpose : To verify the receiver fault tolerance when a short circuit is applied to the receiver inputs.
Note :
Test Setup : Test setup S.
Test Procedure : Apply power to the MAU. Apply a short circuit across the RD circuit for 10 seconds. Verify that when the fault condition is removed the circuit operates normally by performing all other receive tests (Group ID 1411.11).
Conformance : Receivers shall tolerate the application of short circuits between the leads of the RD circuit for an indefinite period of time without damage and shall resume normal operation after such faults are removed.

Test Case ID : 1411.11.02
Test Case Name : RD circuit idle detection.
Status : MANDATORY
Standard Reference : 14.3.1.3.3
PICS Reference : 14.10.4.5.13/8
History :
Test Purpose : To verify that the receiver detects the idle condition.
Note :
Test Setup : Test setup K.
Test Procedure : Apply test signal 14 to the RD circuit of the MAU. Monitor the DI circuit and verify proper start of idle on the DI circuit.
Conformance : The idle condition shall be detected within 2.3 BT of the last low-to-high transition at the receiver.

Test Case ID : 1411.11.03
Test Case Name : RD circuit signal acceptance.
Status : MANDATORY
Standard Reference : 14.3.1.3.1
PICS Reference : 14.10.4.5.8/17, 14.10.4.5.13/1, 14.10.4.5.13/2

History	:	
Test Purpose	:	To verify the receiver differential input voltage acceptance.
Note	:	
Test Setup	:	Test setup K.
Test Procedure	:	Apply test signals 7a-b, 8a-b, 9 and 10 to the RD circuit of the MAU. Monitor the DI circuit and RD circuit. Verify that the pulses appear on the DI circuit.
Conformance	:	Differential signals received on the RD circuit that are within the envelope of Fig 14-16 and 14-17, and have a maximum zero crossing jitter up to ±13.5 ns from the ideal shall be sent to the DI circuit.

Test Case ID	:	1411.11.04
Test Case Name	:	RD circuit differential noise rejection.
Status	:	MANDATORY
Standard Reference	:	14.3.1.3.2
PICS Reference	:	14.10.4.5.13/5-7
History	:	
Test Purpose	:	To verify the receiver noise immunity.
Note	:	
Test Setup	:	Test setup K.
Test Procedure	:	Apply test signals 11a-g, 12a-c and 13a-d to the RD circuit of the MAU. Monitor the DI circuit and RD circuit. For each test signal, verify that the DI circuit remains idle.
Conformance	:	The receiver, while in the Idle state, shall reject as *RD_input* the following signals: (1) All signals which when measured at the output of the following filter would produce a peak magnitude less than 300 mV. The filter is a 3-pole low-pass Butterworth with a 3 dB cut off at 15 MHz. (2) All continuous sinusoidal signals of amplitude less than 6.2 V peak-peak and frequency less than 2 MHz. (3) All sine waves of single cycle duration, starting with phase 0 or 180 degrees, and of amplitude less than 6.2 V peak-peak, where the frequency is between 2 MHz and 15 MHz. For a period of 4 BT before and after this single cycle, the signal shall be less than 300 mV when measured through the filter specified in (1) above.

Test Case ID	:	1411.11.05
Test Case Name	:	RD circuit differential input impedance.
Status	:	MANDATORY
Standard Reference	:	14.3.1.3.4
PICS Reference	:	14.10.4.5.13/9
History	:	
Test Purpose	:	To verify the differential input impedance.
Note	:	
Test Setup	:	Test setup I.
Test Procedure	:	Set the network analyzer to produce 2.5 V peak into 100 Ω. Measure the differential input impedance between 5.0 MHz and 10.0 MHz with 0.5 MHz steps, utilizing a reference resistance of 100 Ω. Calculate the return loss using a reference re-

		sistance of 85 Ω and 111 Ω.
Conformance	:	The differential input impedance shall be such that any reflection, due to differential signals incident upon the RD circuit from a twisted pair having any impedance within the range specified in 14.4.2.2 shall be at least 15 dB below the incident, over the frequency range of 5.0 to 10 MHz.

Test Case ID	:	1411.11.06
Test Case Name	:	RD circuit common mode rejection.
Status	:	MANDATORY
Standard Reference	:	14.3.1.3.5
PICS Reference	:	14.10.4.5.13/10
History	:	
Test Purpose	:	To verify the receiver common mode rejection.
Note	:	
Test Setup	:	Test setup J.
Test Procedure	:	Apply power to the MAU. Apply test signal 15, as differential input signal E_s, to the test fixture such that a 585 mV signal, E_{dif} is present on the RD circuit of the MAU. Monitor the differential input signal, E_{dif}, at the RD circuit of the MAU and the DI circuit. Apply test signal 17 as E_{cm}. Check the DI circuit for the proper state and for jitter.
Conformance	:	Receivers shall assume the proper state on DI for any differential input signal E_s that results in a signal E_{dif} that meets 14.3.1.3.1 even in the presence of common mode voltages E_{cm} (applied as shown in Fig 14-18). E_{cm} shall be a 25 V peak-to-peak square wave, 500 kHz or lower in frequency, with edges no slower than 4 ns (20-80%). Additionally, E_{cm} shall contribute no more than 2.5 ns of edge jitter to the signal transmitted on the DI circuit. The combination of the receiver timing jitter of 14.3.1.3.1 and the common-mode induced jitter are such that the MAU shall add no more then 4.0 ns of edge jitter to E_s before sending the signal on the DI circuit.

Test Case ID	:	1411.11.07
Test Case Name	:	RD circuit link test pulse acceptance.
Status	:	MANDATORY
Standard Reference	:	14.3.1.3.2
PICS Reference	:	14.10.4.5.13/4
History	:	
Test Purpose	:	To verify the receiver acceptance of link test pulses.
Note	:	
Test Setup	:	Test setup B.
Test Procedure	:	Apply power to the MAU. Monitor the DI circuit and TD circuit. Stop any input on the RD circuit for at least 10 seconds. Check that the MAU is in a Link Test Fail state. Start sending link test pulses on the RD circuit. The link test pulses shall occur within 25 - 150 ms of each other and have shape and amplitude as described below. After at least 10 link test pulses, immediately apply test signal 1 to the DO circuit of the MAU and check that the MAU has entered the Link Test Pass state by monitoring the signals on the TD circuit.

		The link test pulses used shall have the following characteristics: (1) As in Fig 14-12 with a peak amplitude of 585 mV, a pulsewidth of 0.60 BT and maximum undershoot. (2) As in Fig 14-12 with maximum allowed amplitude and pulsewidth.
Conformance	:	The receiver when presented with a signal meeting the requirements of 14.2.1.1 and within the envelope of Fig 14-12 shall accept it as a link test pulse.

Test Case ID	:	1411.11.08
Test Case Name	:	Received signal added jitter.
Status	:	MANDATORY
Standard Reference	:	14.3.1.3.1
PICS Reference	:	14.10.4.5.13/3
History	:	
Test Purpose	:	To verify that jitter added by MAU receiver does not exceed ±1.5 ns.
Note	:	
Test Setup	:	Test setup H.
Test Procedure	:	Apply power to the MAU. Apply test signal 16 to the RD circuit of the MAU. Monitor the DI circuit and RD circuit. Using the oscilloscope, measure the jitter of the zero crossings. Disregard the first bit sent on the DI circuit. Set the oscilloscope to trigger on the RD circuit signal zero crossing with positive slope. Observe the zero crossings 8 and 8.5 BT from the triggering zero crossing. An external MAU is compliant when all zero crossings fall within the time intervals 8.0 BT ± 3 ns and 8.5 BT ± 3 ns.
Conformance	:	The MAU receiver shall add no more than ±1.5 ns jitter to the received signal before sending the signal to the DI circuit.

Test Case ID	:	1411.11.09
Test Case Name	:	Receiver fault tolerance, impulse.
Status	:	MANDATORY
Standard Reference	:	14.3.1.3.6
PICS Reference	:	14.10.4.5.13/12
History	:	
Test Purpose	:	To verify the receiver fault tolerance when a high voltage impulse is applied to the receiver.
Note	:	The impulse shape should be adjusted while applied to the test object as per IEC Publication 60 [8].
Test Setup	:	Test setup BB.
Test Procedure	:	Apply a IEC standard full impulse voltage of positive polarity, with a peak value of 1000 V, a virtual front time of 300 ns and virtual time to half value of 50 µs as E_{cm} to the test setup. Repeat the test using a negative polarity impulse. Verify that the receiver still operates normally by performing the receiver test group tests (group ID 1411.11).
Conformance	:	Receivers shall withstand without damage a 1000 V common-mode impulse of either polarity ($E_{impulse}$ as indicated in Fig 14-19). The shape of the impulse shall be 0.3/50 µs (300 ns virtual

front time, 50 μs virtual time of half value), as defined in IEC Publication 60 [8].

6.2.1.12 T est Group 141 1.12 - AUI Signal Characteristics

Test Group ID	:	1411.12
Test Group Name	:	AUI Signal Characteristics.
Test Group Purpose	:	To ensure correct signaling characteristics of the AUI.

Test Case ID	:	1411.12.01
Test Case Name	:	Labeled signaling rate.
Status	:	CONDITIONAL (Only tested if the AUI is implemented and available for testing).
Standard Reference	:	7.3.2
PICS Reference	:	14.10.4.6.1/1
History	:	
Test Purpose	:	To verify that the MAU is correctly labeled with the actual signaling rate used with that device.
Note	:	
Test Setup	:	None.
Test Procedure	:	Visually check the MAU label for an indication that the signalling rate is 10 Mb/s.
Conformance	:	To facilitate the configuration of operational systems, DTE and MAU devices shall be labeled with the actual signaling rate used with that device.

Test Case ID	:	1411.12.02
Test Case Name	:	CS0 signal frequency (on CI).
Status	:	CONDITIONAL (Only tested if the AUI is implemented and available for testing).
Standard Reference	:	7.3.1.2
PICS Reference	:	14.10.4.6.1/2
History	:	
Test Purpose	:	To verify the frequency of the CS0 signal.
Note	:	
Test Setup	:	Test setup C.
Test Procedure	:	Apply test signal 3b to the DO circuit of the MAU. Monitor the CI circuit. Measure the frequency of the CS0 signal.
Conformance	:	The tolerance ... on CI ... is BR ± 15%.

Test Case ID	:	1411.12.03
Test Case Name	:	CS0 signal duty cycle.
Status	:	CONDITIONAL (Only tested if the AUI is implemented and available for testing).
Standard Reference	:	7.3.1.2
PICS Reference	:	14.10.4.6.1/3
History	:	
Test Purpose	:	To verify the duty cycle of the CS0 signal.
Note	:	
Test Setup	:	Test setup C.
Test Procedure	:	Apply test signal 3b to the DO circuit of the MAU. Monitor the

		CI circuit. Measure the duty cycle of the CS0 signal.
Conformance	:	The nominal duty cycle is 50/50 and shall be no worse than 60/40.

6.2.1.13 Test Group 1411.13 - DI and CI Driver Characteristics

Test Group ID	:	1411.13
Test Group Name	:	DI and CI Driver Characteristics.
Test Group Purpose	:	To ensure correct operation of the AUI DI and CI drivers.

Test Case ID	:	1411.13.01
Test Case Name	:	AUI driver differential output voltage.
Status	:	CONDITIONAL (Only tested if the AUI is implemented and available for testing).
Standard Reference	:	7.4.1.1
PICS Reference	:	14.10.4.6.2/1-4
History	:	802.3/CR005, CTTF/CR3, CTTF/CR4
Test Purpose	:	To verify the correct differential output voltage.
Note	:	T_j = 4 ns [2 $\times$ (1.5 ns MAU-DTE jitter + 0.5 ns source jitter)].
Test Setup	:	Test setup U.
Test Procedure	:	Using a test load of 73 $\Omega \pm 1\%$ in parallel with 50 $\mu H \pm 1\%$, monitor the CI circuit and DI circuit of the MAU under test. Monitor the current into the test loads. Apply test signal 1 to the DO circuit of the MAU under test. Apply test signal 1 to the DO circuit of the tester MAU to create a collision.

(1) During collision, verify that the signals on the CI circuit and DI circuit meet the requirements of Fig 7-11 by using the following procedure. Construct a template representing the shaded area of Fig 7-11 using the zero crossings as reference points. Once constructed, the template may be shifted along the time axis in order to accommodate differences in the 10% to 50% and 50% to 90% transition times. Verify that time T_2 is BT $\pm$ 4 ns or BT/2 $\pm$ 4 ns. Find the peak value of V_{dm}. This is V_{max}. Find the minimum value of V_{dm} during the period between the shaded regions for the waveform's rising and falling transitions (time T1 in Fig 7-11). This minimum value is V_{min}. Verify that V_{max} is less than 1315 mV, that V_{min} is greater than 450 mV and that V_{max}/V_{min} is less than 1.37. Measure the V_{dm} 24 ns after the zero crossing and verify that it remains less than 1170 mV and within the template.

(2) Observe the DI circuit signals for 2 bit times after the last low to high transition of the packet. Verify that the differential output voltage is at least 380 mV during that time.

(3) Observe the DI circuit signals 80 bit times after the last low to high transition of the packet. Verify that the output voltage is $\leq \pm 40$ mV differential and the current into the load is $\leq$ 4 mA.

(4) Observe the CI circuit signals for 2 bit times after the last low to high transition of CS0. Verify that the differential output voltage is at least 380 mV during that

time.

(5) Observe the CI circuit signals 80 bit times after the last low to high transition of CS0. Verify that the output voltage is $\leq \pm 40$ mV differential and the current into the load is ≤ 4 mA.

Repeat the test using a test load of 83 Ω ± 1% in parallel with 50 µH ± 1%.

Conformance : The following conformance statements are applicable as noted.

(1) For (1) above: The value of V_{dm} into either of the two test loads identified above (R = 73 Ω or 83 Ω ± 1%) at the interface connector of the driving unit shall satisfy conditions defined by values V_{min} and V_{max} shown in Fig 7-11 for signals in between BR and BR/2 meeting the frequency and duty cycle tolerances specified for the signal being driven. V_{max} shall be < 1315 mV, V_{min} shall be > 450 mV, V_{max}/V_{min} shall be < 1.37. V_{dm} shall remain < 1170 mV 24 ns after a zero crossing. The waveform shall remain within the shaded area limits.

(2) For (2) through (5): When a driver, connected to the appropriate two test loads identified above, enters the idle state, it shall maintain a minimum differential output voltage of at least 380 mV for at least 2 bit times after the last low to high transition. The driver differential output voltage shall then approach within 40 mV of 0 V within 80 bit times. In addition, the current into the appropriate test load shall be limited in magnitude to 4 mA within 80 bit times. Undershoot, if any, upon reaching 0 V shall be limited to -100 mV. See Fig 7-12.

Test Case ID : 1411.13.02

Test Case Name : AUI driver requirements after idle.

Status : CONDITIONAL (Only tested if the AUI is implemented and available for testing).

Standard Reference : 7.4.1.2

PICS Reference : 14.10.4.6.2/5

History : CTTF/CR3, CTTF/CR4, CTTF/CR9

Test Purpose : To verify the signal characteristics of the first bit transmitted after idle.

Note :

Test Setup : Test setup U.

Test Procedure : Using a test load of 73 Ω ± 1% in parallel with 50 µH ± 1%, monitor the CI circuit and DI circuit of the MAU under test. Apply test signal 1 to the DO circuit of the MAU under test. Apply test signal 1 to the DO circuit of the tester MAU to create a collision. Verify that the second bit transmitted on the DI circuit and CI circuit meets the requirements of 7.4.1.1 and Fig 7-11. Repeat the test using a test load of 83 Ω ± 1% in parallel with 50 µH ± 1%.

Conformance : When the driver becomes nonidle after a period of idle on the interface circuit, the differential output voltage at the interface connector shall meet the requirements of 7.4.1.1 beginning with the second bit transmitted. The first bit send over the driver circuit may contain phase violations or invalid data.

Test Case ID	:	1411.13.03
Test Case Name	:	AUI driver common mode output voltage, ac.
Status	:	CONDITIONAL (Only tested if the AUI is implemented and available for testing).
Standard Reference	:	7.4.1.3
PICS Reference	:	14.10.4.6.2/6
History	:	CTTF/CR1
Test Purpose	:	To verify the ac common mode output voltage of the AUI drivers.
Note	:	The balance of the test equipment (such as the matching of the 39 Ω resistors) must exceed that required of the transmitter.
Test Setup	:	Test setup EE.
Test Procedure	:	Apply test signals 4 and 25 to the DO circuit of the MAU under test. In each case, apply test signal 1 to the DO circuit of the tester MAU to create a collision. Measure the ac common mode output voltage E_{cm} on the DI circuit and CI circuit of the MAU under test using Filter 1, then Filter 2. The filter is connected across the circuit under test (DI or CI) and circuit VC.
Conformance	:	The magnitude of the ac component of the common mode output voltage of the driver, measured between the midpoint of a test load consisting of a pair of matched 39 Ω ± 1% resistors and circuit VC, as shown in Fig 7-13, shall not exceed 2.5 V peak from 30 Hz to 40 kHz and 160 mV peak from 40 kHz to BR.

Test Case ID	:	1411.13.04
Test Case Name	:	AUI driver differential output voltage, open circuit.
Status	:	CONDITIONAL (Only tested if the AUI is implemented and available for testing).
Standard Reference	:	7.4.1.4
PICS Reference	:	14.10.4.6.2/7
History	:	
Test Purpose	:	To verify the open circuit differential output voltage.
Note	:	
Test Setup	:	Test setup W.
Test Procedure	:	Apply test signal 1 to the DO circuit of the MAU under test. Apply test signal 1 to the DO circuit of the tester MAU to create a collision. Measure the open circuit differential output voltage, E_{dif}, on the DI circuit and CI circuit of the MAU under test.
Conformance	:	The differential output voltage into an open circuit, measured at the interface connector of the driving unit, shall not exceed 13 V peak.

Test Case ID	:	1411.13.05
Test Case Name	:	AUI driver common mode output voltage, dc.
Status	:	CONDITIONAL (Only tested if the AUI is implemented and available for testing).
Standard Reference	:	7.4.1.5
PICS Reference	:	14.10.4.6.2/8
History	:	
Test Purpose	:	To verify the dc common mode output voltage of the AUI driv-

		ers.
Note	:	The balance of the test equipment (such as the matching of the 39 Ω resistors) must exceed that required of the transmitter.
Test Setup	:	Test setup V.
Test Procedure	:	Apply test signal 1 to the DO circuit of the MAU under test. Apply test signal 1 to the DO circuit of the tester MAU to create a collision. Measure the dc common mode output voltage E_{cm} on the DI circuit and CI circuit of the MAU under test.
Conformance	:	The magnitude of the dc component of the common mode output voltage of the driver, measured between the midpoint of a test load consisting of a pair of matched 39 Ω ± 1% resistors and circuit VC, as shown in Fig 7-13, shall not exceed 5.5 V.

Test Case ID	:	1411.13.06
Test Case Name	:	AUI driver fault tolerance while idle.
Status	:	CONDITIONAL (Only tested if the AUI is implemented and available for testing).
Standard Reference	:	7.4.1.6
PICS Reference	:	14.10.4.6.2/9, 14.10.4.6.2/10
History	:	
Test Purpose	:	To verify the AUI driver fault tolerance when idle.
Note	:	
Test Setup	:	Test setup X.
Test Procedure	:	Monitor the current output of the switch A lead and switch B lead.

(1) Connect the switch A and switch B leads to the DI-A and DI-B outputs of the MAU under test. Apply the various fault conditions (see below), in turn, for 10 seconds each and observe that when all fault conditions are removed, the circuit operates normally by performing tests 1411.13.01 through 1411.13.05 inclusive. Verify that the output current on either terminal of the differential output under any fault condition is less then or equal to 150 mA.

(2) Connect the switch A and switch B leads to the CI-A and CI-B outputs of the MAU under test. Apply the various fault conditions (see below), in turn, for 10 seconds each and observe that when all fault conditions are removed, the circuit operates normally by performing tests 1411.13.01 through 1411.13.05 inclusive. Verify that the output current on either terminal of the differential output under any fault condition is less than or equal to 150 mA.

Fault	**Switch Settings**	
Condition	**Lead A**	**Lead B**
1	1	1
2	4	3
3	3	4
4	4	4
5	2	3
6	3	2
7	2	2
8	3	3

Conformance	:	Any single driver in the interface, when idle or driving any permissible signal, shall tolerate the application of each of the faults specified by the switch settings in Fig 7-14 indefinitely; and after the fault condition is removed, the operation of the driver, according to the specifications of 7.4.1.1 through 7.4.1.5, shall not be impaired. In addition, the magnitude of the output current from either output of the driver under any of the fault conditions specified shall not exceed 150 mA.

Test Case ID	:	1411.13.07
Test Case Name	:	AUI driver fault tolerance while active.
Status	:	CONDITIONAL (Only tested if the AUI is implemented and available for testing).
Standard Reference	:	7.4.1.6
PICS Reference	:	14.10.4.6.2/9, 14.10.4.6.2/10
History	:	
Test Purpose	:	To verify the transmitter fault tolerance when active.
Note	:	
Test Setup	:	Test setup X.
Test Procedure	:	Monitor the current output of the switch A lead and switch B lead.

(1) Connect the switch A and switch B leads to the DI-A and DI-B outputs of the MAU under test. Apply test signal 4 to the DO circuit of the MAU under test. Apply the various fault conditions (see below), in turn, for 10 seconds each and observe that when all fault conditions are removed, the circuit operates normally by performing tests 1411.13.01 through 1411.13.05 inclusive. Verify that the output current on either terminal of the differential output under any fault condition is less than or equal to 150 mA.

(2) Connect the switch A and switch B leads to the CI-A and CI-B outputs of the MAU under test. Apply test signal 3a to the DO circuit of the MAU under test. Apply the various fault conditions (see below), in turn, for 10 seconds each and observe that when all fault conditions are removed, the circuit operates normally by performing tests 1411.13.01 through 1411.13.05 inclusive. Verify that the output current on either terminal of the differential output under any fault condition is less than or equal to 150 mA.

Fault Condition	**Switch Settings Lead A**	**Lead B**
1	1	1
2	4	3
3	3	4
4	4	4
5	2	3
6	3	2
7	2	2
8	3	3

Conformance	:	Any single driver in the interface, when idle or driving any per-

missible signal, shall tolerate the application of each of the faults specified by the switch settings in Fig 7-14 indefinitely; and after the fault condition is removed, the operation of the driver, according to the specifications of 7.4.1.1 through 7.4.1.5, shall not be impaired.
In addition, the magnitude of the output current from either output of the driver under any of the fault conditions specified shall not exceed 150 mA.

6.2.1.14 Test Group 1411.14 - DO Receiver Characteristics

Test Group ID	:	1411.14
Test Group Name	:	DO Receiver Characteristics.
Test Group Purpose	:	To ensure correct operation of the AUI DO circuit.

Test Case ID	:	1411.14.01
Test Case Name	:	DO receiver threshold when unsquelched.
Status	:	CONDITIONAL (Only tested if the AUI is implemented and available for testing).
Standard Reference	:	7.4.2.1
PICS Reference	:	14.10.4.6.3/1
History	:	
Test Purpose	:	To verify the DO receiver sensitivity.
Note	:	*This parameter is not directly testable because the receiver state is not directly observable and is immaterial if the DO circuit remains in the squelched state. Even though testing for compliance is not practical, conformance to the standard,* ***by design****, is the responsibility of the manufacturer with compliance status to be noted in the PICS.*
Test Setup	:	
Test Procedure	:	
Conformance	:	When the receiving interface circuit at the interface connector of the receiving equipment is driven by a differential input signal at either BR or BR/2 meeting the frequency and duty cycle tolerances specified for the receiving circuit, when the A lead is 160 mV positive with respect to the B lead, the interface is in the HI state, and when the A lead is 160 mV negative with respect to the B lead, the interface circuit is in the LO state. The receiver output shall assume the intended HI and LO states for the corresponding input conditions.

Test Case ID	:	1411.14.02
Test Case Name	:	DO receiver threshold while in the Idle state.
Status	:	CONDITIONAL (Only tested if the AUI is implemented and available for testing).
Standard Reference	:	14.3.2.1
PICS Reference	:	14.10.4.6.3/2
History	:	
Test Purpose	:	To verify the DO receiver squelching.
Note	:	
Test Setup	:	Test setup B.
Test Procedure	:	Apply test signal 20 to the DO circuit of the MAU. Monitor the

		TD circuit. Monitor the TD circuit for correct state.
Conformance	:	Additionally, the AUI DO receiver, while in the Idle state, shall reject an input waveform of less than ±160 mV differential.

Test Case ID	:	1411.14.03
Test Case Name	:	High to idle transition on DO circuit.
Status	:	CONDITIONAL (Only tested if the AUI is implemented and available for testing).
Standard Reference	:	7.4.1.1, 14.3.1.2.1
PICS Reference	:	14.10.4.6.3/3
History	:	
Test Purpose	:	To verify that the DO receiver correctly recognizes idle.
Note	:	
Test Setup	:	Test setup D, using Load 1 of Fig 14-11.
Test Procedure	:	Apply test signal 23a to the DO circuit of the MAU. Monitor the TD circuit. Verify that the idle signal matches the template of Fig 14-10. Repeat the test using test signal 23b.
Conformance	:	The receiving unit shall take precautions to ensure that a HI to idle transition is not falsely interpreted as an idle to nonidle transition, even in the presence of signal droop due to ac coupling in the interface driver or receiver circuits.

Test Case ID	:	1411.14.04
Test Case Name	:	DO circuit differential input impedance.
Status	:	CONDITIONAL (Only tested if the AUI is implemented and available for testing).
Standard Reference	:	7.4.2.2
PICS Reference	:	14.10.4.6.3/4
History:	:	
Test Purpose	:	To verify the input impedance of the DO receiver.
Note	:	
Test Setup	:	Test setup Y.
Test Procedure	:	Using the network analyzer, measure the input impedance (magnitude and phase) of the DO circuit of the MAU at a frequency of 10 MHz and an amplitude of 500 mV.
Conformance	:	The ac differential input impedance for AUI receivers located in MAUs shall have a real part of 77.83 Ω ± 6%, with the sign of the imaginary part positive, and the phase angle of the impedance in degrees ≤ 0.0338 times the real part of the impedance when measured with a 10 MHz sine wave.

Test Case ID	:	1411.14.05
Test Case Name	:	DO circuit common mode range, ac.
Status	:	CONDITIONAL (Only tested if the AUI is implemented and available for testing).
Standard Reference	:	7.4.2.3
PICS Reference	:	14.10.4.6.3/5
History	:	CTTF/CR2
Test Purpose	:	To verify the AUI DO receiver ac common mode range.
Note	:	Proper output state implies correct polarity with respect to input data. Set the required voltage at the function generator be-

		fore connecting it to the test setup.
Test Setup	:	Test setup Z.
Test Procedure	:	Apply test signal 6, as differential input signal E_s, to the test fixture. Monitor the differential input signal E_{dif} at the DO circuit of the MAU and the TD circuit. In succession, apply test signals 21a through 21g as E_{cm}. Check the TD circuit for proper state.
Conformance	:	When the receiving interface circuit at the receiving equipment is driven by a differential input signal at either BR or BR/2 meeting the frequency and duty cycle tolerances specified for the circuit being driven, the receiver output shall assume the proper output state as specified in 7.4.2.1, in the presence of a peak common mode ac sine wave voltage either of from 30 Hz to 40 kHz referenced to circuit VC in magnitude from 0 to 3 V, or in magnitude 0 to 200 mV for ac voltages of from 40 kHz to BR as shown in Fig 7-15.

Test Case ID	:	1411.14.06
Test Case Name	:	DO circuit total common mode range.
Status	:	CONDITIONAL (Only tested if the AUI is implemented and available for testing).
Standard Reference	:	7.4.2.4
PICS Reference	:	14.10.4.6.3/6, 14.10.4.6.3/7
History	:	CTTF/CR2
Test Purpose	:	To verify the AUI DO receiver total common mode range and common mode current limit.
Note	:	Proper output state implies correct polarity with respect to input data. Set the required voltage at the function generator before connecting it to the test setup.
Test Setup	:	Test setup Z.
Test Procedure	:	Apply test signal 6, as differential input signal E_s, to the test fixture. Monitor the differential input signal E_{dif} at the DO circuit of the MAU and the TD circuit. In succession, apply test signals 22a through 22n as E_{cm}. Check the TD circuit for proper state.
Conformance	:	When the receiving interface circuit at the receiving equipment is driven by a differential input signal at either BR or BR/2 meeting the frequency and duty cycle tolerances specified for the circuit being driven, the receiver output shall assume the proper output state as specified in 7.4.2.1, in the presence of a total common mode voltage, dc plus ac, referenced to circuit VC in magnitude from 0 to 5.5 V, as shown in the test setup of Fig 7-15. The AC component shall not exceed the requirements of 7.4.2.3. The receiver shall be so designed that the magnitude of the current from the common mode voltage source used in the test shall not exceed 1 mA.

Test Case ID	:	1411.14.07
Test Case Name	:	IDL detection, DO circuit.
Status	:	CONDITIONAL (Only tested if the AUI is implemented and available for testing).

Standard Reference	:	7.3.1.1, 14.3.1.2.1
PICS Reference	:	14.10.4.6.3/8
History	:	
Test Purpose	:	To verify AUI DO receiver IDL detection.
Note	:	A MAU that passes test case 1411.14.03 is considered conformant.
Test Setup	:	Test setup D, using Load 1 of Fig 14-11.
Test Procedure	:	Apply test signal 23a to the DO circuit of the MAU. Monitor the TD circuit. Verify that the idle signal matches the template of Fig 14-10. Repeat the test using test signal 23b.
Conformance	:	The IDL condition shall be detected within 1.6 bit times at the receiving device.

Test Case ID	:	1411.14.08
Test Case Name	:	Requirements after idle, DO circuit.
Status	:	CONDITIONAL (Only tested if the AUI is implemented and available for testing).
Standard Reference	:	7.4.2.5, 14.2.1.1
PICS Reference	:	14.10.4.6.3/9
History	:	
Test Purpose	:	To verify that the AUI DO receiver stabilizes within 2 BT.
Note	:	From an external perspective it is difficult to separate the internal effects of the AUI receive circuit (DO) and those of the MAU TD circuit, thus if test cases 1411.01.02 and 1411.01.03 pass, then the DO receiver is assumed to be in conformance.
Test Setup	:	Test setup A.
Test Procedure	:	Perform tests 1411.01.02 and 1411.01.03.
Conformance	:	The conformance statements of 1411.01.02 and 1411.01.03 shall apply in addition to the following: When the receiver becomes nonidle after a period of idle on the interface circuit, the characteristics of the signal at the output of the receiver shall stabilize within the startup delay allowed for the device incorporating the receiver so that it is not prevented from meeting the jitter specifications established for that device.

Test Case ID	:	1411.14.09
Test Case Name	:	DO circuit fault tolerance.
Status	:	CONDITIONAL (Only tested if the AUI is implemented and available for testing).
Standard Reference	:	7.4.2.6
PICS Reference	:	14.10.4.6.3/10, 14.10.4.6.3/11
History	:	
Test Purpose	:	To verify receiver fault tolerance.
Note	:	
Test Setup	:	Test setup X.
Test Procedure	:	Monitor the current output of the switch A lead and switch B lead. Disconnect the TPG from the DO circuit of the MAU under test. Connect the switch A and switch B leads to the DO-A and DO-B inputs of the MAU under test. Apply the various fault conditions (see below), in turn, for 10 seconds each and observe that when all fault conditions are removed, the circuit operates normally by performing tests 1411.14.01 through

1411.14.08 inclusive. Verify that the input current on either terminal of the differential input under any fault condition is less than or equal to 3 mA.

Fault Condition	**Switch Settings Lead A**	**Lead B**
1	1	1
2	4	3
3	3	4
4	4	4
5	2	3
6	3	2
7	2	2
8	3	3

Conformance : Any single receiver in the interface shall tolerate the application of each of the faults specified by the switch settings in Fig 7-16 indefinitely, and after the fault condition is removed, the operation of the receiver according to the specifications of 7.4.2.1 through 7.4.2.6 shall not be impaired.
In addition, the magnitude of the current into either input of the receiver under any of the fault conditions specified shall not exceed 3 mA.

6.2.1.15 Test Group 1411.15 - Power Consumption

Test Group ID : 1411.15
Test Group Name : Power Consumption.
Test Group Purpose : To ensure that the power consumption is not excessive.

Test Case ID : 1411.15.01
Test Case Name : Power surge limitation and duration.
Status : CONDITIONAL (Only tested if the AUI is implemented and available for testing).
Standard Reference : 14.3.2.3
PICS Reference : 14.10.4.6.4/1, 14.10.4.6.4/2
History :
Test Purpose : To verify the power-on surge current characteristics.
Note :
Test Setup : Test setup A.
Test Procedure : Monitor the current in the VP circuit of the MAU. Measure the peak surge current, I_p, and the duration, T_w, during which the current exceeds the larger of 0.5 A or $0.5 \times I_p$.
Conformance : Following power-on, the surge current drawn by the MAU shall be such that $I_p \times T_w$ is less than or equal to 2×10^{-3} ampere-seconds, where I_p is the peak surge current and T_w is the time during which the current exceeds the larger of 0.5A or $0.5 \times I_p$.

Test Case ID : 1411.15.02
Test Case Name : Steady state current.
Status : CONDITIONAL (Only tested if the AUI is implemented and available for testing).
Standard Reference : 14.3.2.3
PICS Reference : 14.10.4.6.4/3

History	:	
Test Purpose	:	To verify the steady state current characteristics.
Note	:	
Test Setup	:	Test setup A.
Test Procedure	:	Monitor the current in the VP circuit of the MAU. Measure the current drawn by the MAU 100 ms following the application of power. Continue monitoring the VP current while applying test signal 5 to the DO circuit of the MAU.
Conformance	:	After 100 ms following power-on, the current drawn by the MAU shall not exceed 0.5 A when powered by the AUI.

Test Case ID	:	1411.15.03
Test Case Name	:	Voltage source range and current limited supplies.
Status	:	CONDITIONAL (Only tested if the AUI is implemented and available for testing).
Standard Reference	:	14.3.2.3, 7.5.2.5
PICS Reference	:	14.10.4.6.4/4, 14.10.4.6.4/5
History	:	
Test Purpose	:	To verify proper operation with current limited sources.
Note	:	
Test Setup	:	As specified in the individual test cases.
Test Procedure	:	Set the current limit control on the power supply to limit at 500 mA. Perform test cases 1411.01.01 through 1411.01.06, 1411.02.01 through 1411.02.05, 1411.13.01 through 1411.13.05, and 1411.14.01 through 1411.14.06.
Conformance	:	The following conformance statements apply: (1) The MAU shall be capable of operating from all possible voltage sources, including those current limited to 0.5A, as supplied by the DTE or repeater through the resistance of all permissible AUI cables. (2) The Voltage Plus (VP) circuit is an optional circuit that may be sourced from the DTE. If this circuit is sourced from the DTE it shall be capable of operating at one fixed level between +12 V dc -6% and +15 V dc +5% with respect to circuit VC for all current from 0 to 500 mA.

Test Case ID	:	1411.15.04
Test Case Name	:	Power cycle and low VP circuit behavior.
Status	:	CONDITIONAL (Only tested if the AUI is implemented and available for testing).
Standard Reference	:	14.3.2.3, 7.5.2.5
PICS Reference	:	14.10.4.6.4/6, 14.10.4.6.4/7
History	:	
Test Purpose	:	To verify proper operation with low voltage sources and power cycling.
Note	:	Extraneous signal on the TD circuit is defined to be greater than ±50 mV; extraneous signal on the CI and DI circuits is defined to be greater than ±40 mV.
Test Setup	:	Test setup A.
Test Procedure	:	Monitor the TD circuit, CI circuit and DI circuit of the MAU. (1) Turn the power to MAU off then on several times. Ver-

ify that no extraneous signals appear on the TD, CI or DI circuits.

(2) Apply power to the MAU then adjust the voltage on circuit VP from +15.75 V down to 0.25 V in 0.5 V steps at a rate of change of 1 step per second. Adjust the voltage from 0.25 V to +15.75 V in 0.5 V steps at a rate of change of 1 step per second. At each step ensure that no extraneous signals are introduced on the TD circuit.

Conformance : The following conformance statements apply:

(1) The MAU shall not introduce extraneous signals on the TD, CI, or DI circuits during normal power-up and power-down.

(2) MAU designers are cautioned that protection means employed by power sources may cause the voltage at signal VP to drop below the minimum operational voltage specified without going completely to zero volts when loads drawing in excess of the current supplied are applied between VP and VC. Adequate provisions shall be made to ensure that such a condition does not cause the MAU to disrupt the medium.

6.2.1.16 Test Group 1411.16 - Circuit Termination

Test Group ID : 1411.16
Test Group Name : Circuit Termination.
Test Group Purpose : To ensure that the circuit terminations have the proper impedance and coupling to circuit VC.

Test Case ID : 1411.16.01
Test Case Name : Impedance and coupling to circuit VC.
Status : CONDITIONAL (Only tested if the AUI is implemented and available for testing).
Standard Reference : 7.5.2.8
PICS Reference : 14.10.4.6.5/2, 14.10.4.6.5/3
History :
Test Purpose : To verify that the circuit shield pins are capacitively coupled to VC with an impedance magnitude of < 5 Ω.
Note :
Test Setup : Test setup Y, with the network analyzer connected as in the test procedure.
Test Procedure : Using the network analyzer, measure the impedance between pins 1, 4, 11 and 14 and pin VC at a frequency of 5 MHz. Verify that the magnitude of the impedance is less than 5 Ω and the phase angle is -90° ± 20°.
Conformance : Individual pin terminations shall meet the following requirements:

(1) Pins 1, 4, 11, 14 connected to logic ground in the DTE
(2) Pins 1, 4, 11, 14 capacitively coupled to VC in MAU
(3) Impedance to ground < 5 Ω at lowest operational BR/2 in the MAU and at highest BR in the DTE.

Test Case ID : 1411.16.02

Test Case Name	:	Common-mode termination.
Status	:	CONDITIONAL (Only tested if the AUI is implemented and available for testing).
Standard Reference	:	7.5.2.6
PICS Reference	:	14.10.4.6.5/1
History	:	
Test Purpose	:	To verify that all common-mode terminations are made with respect to circuit VC.
Note	:	*This test case is considered untestable. Due to the different possible methods of termination, it is not practical to measure or test. Even though testing for compliance is not practical, conformance to the standard by design is the responsibility of the manufacturer with compliance status to be noted in the PICS.*
Test Setup	:	
Test Procedure	:	
Conformance	:	Also, all common-mode terminators for AUI circuits shall be made to circuit VC.

6.2.1.17 Test Group 1411.17 - Safety Requirements

Test Group ID	:	1411.17
Test Group Name	:	Safety Requirements.
Test Group Purpose	:	To verify general safety.

Test Case ID	:	1411.17.01
Test Case Name	:	Safety Grounding Path.
Status	:	CONDITIONAL (Only tested if the AUI is implemented and available for testing).
Standard Reference	:	14.7.2.2
PICS Reference	:	14.10.4.5.15/1
History	:	
Test Purpose	:	To verify presence of a safety grounding path.
Note	:	*The details of this test procedure are beyond the scope of this document. See the PIXIT or applicable standard(s) for further information.*
Test Setup	:	
Test Procedure	:	
Conformance	:	Any safety grounding path for the MAU shall be provided through the circuit PG of the AUI connection.

Test Case ID	:	1411.17.02
Test Case Name	:	General Safety.
Status	:	MANDATORY.
Standard Reference	:	14.7.1
PICS Reference	:	14.10.4.5.15/3
History	:	
Test Purpose	:	To verify conformance to IEC 380, 435 or 950.
Note	:	*The details of this test procedure are beyond the scope of this document. See the PIXIT or applicable standard(s) for further information.*
Test Setup	:	
Test Procedure	:	

Conformance	:	All equipment meeting this standard shall conform to one of the following IEC Publications: 380, 435, or 950.

Test Case ID	:	1411.17.03
Test Case Name	:	Application of Telephony Voltages.
Status	:	MANDATORY.
Standard Reference	:	14.7.2.4
PICS Reference	:	14.10.4.5.15/4
History	:	
Test Purpose	:	To verify no safety hazard exists when telephony voltages are applied.
Note	:	*The details of this test procedure are beyond the scope of this document. See the PIXIT or applicable standard(s) for further information.*
Test Setup	:	
Test Procedure	:	
Conformance	:	Although 10BASE-T equipment is not required to survive such wiring hazards without damage, application of any of the above voltages shall not result in any safety hazard.

6.2.2 Basic Interconnection Test Group

6.2.2.1 Test Group 1411.18 - Mechanical Characteristics, MDI

Test Group ID	:	1411.18
Test Group Name	:	Mechanical Characteristics, MDI.
Test Group Purpose	:	To ensure that the proper MDI connector is installed.

Test Case ID	:	1411.18.01
Test Case Name	:	MDI connector.
Status	:	MANDATORY.
Standard Reference	:	14.5.1
PICS Reference	:	14.10.4.5.14/1
History	:	
Test Purpose	:	To verify the MDI connector configuration and dimensions.
Note	:	
Test Setup	:	None.
Test Procedure	:	Visually check the connector type and gender. Verify that the connector is an eight-pin jack as per ISO 8877 [10].
Conformance	:	Eight-pin connectors meeting the requirements of Section 3 and Figures 1-5 of ISO 8877 shall be used as the mechanical interface to the twisted-pair segment. The plug connector shall be used on the twisted-pair link segment and the jack on the MAU.

Test Case ID	:	1411.18.02
Test Case Name	:	MDI connector contact assignment.
Status	:	MANDATORY.
Standard Reference	:	14.5.1
PICS Reference	:	14.10.4.5.14/2-6
History	:	

Test Purpose	:	To verify the MDI connector contact assignment.
Note	:	
Test Setup	:	None.
Test Procedure	:	Check that the MDI connector has the pin assignment shown in the table below.
Conformance	:	The following table shows the assignment of signals to connector contacts.

Contact	MDI Signal
1	TD+
2	TD-
3	RD+
6	RD-

Test Case ID	:	1411.18.03
Test Case Name	:	Crossover function indication.
Status	:	CONDITIONAL (Only tested if the crossover function is implemented).
Standard Reference	:	14.5.2
PICS Reference	:	14.10.4.5.14/7
History	:	
Test Purpose	:	To verify proper connector marking when the crossover function is implemented.
Note	:	
Test Setup	:	None.
Test Procedure	:	Visually check the connector for the presence of a “X”.
Conformance	:	Additionally, the MDI connector for a MAU that implements the crossover function shall be marked with a graphical symbol “X”.

Test Case ID	:	1411.18.04
Test Case Name	:	MDI-X connector contact assignment.
Status	:	CONDITIONAL (Only tested if the crossover function is implemented).
Standard Reference	:	14.5.2
PICS Reference	:	14.10.4.5.14/8-11
History	:	
Test Purpose	:	To verify the MDI connector contact assignment when the crossover function is implemented.
Note	:	
Test Setup	:	None.
Test Procedure	:	Check that the MDI connector has the pin assignment shown in the table below.
Conformance	:	The following table shows the assignment of signals to connector contacts.

Contact	MDI Signal
1	RD+
2	RD-
3	TD+
6	TD-

6.2.2.2 Test Group 1411.19 - Mechanical Characteristics, AUI

Test Group ID	:	1411.19
Test Group Name	:	Mechanical Characteristics, AUI.
Test Group Purpose	:	To ensure that the proper AUI connector is installed.

Test Case ID	:	1411.19.01
Test Case Name	:	AUI connector physical dimensions.
Status	:	CONDITIONAL (Only tested if the AUI is implemented and available for testing).
Standard Reference	:	7.6.1, 7.6.2
PICS Reference	:	14.10.4.6.6/1
History	:	
Test Purpose	:	To verify the AUI connector configuration and dimensions.
Note	:	
Test Setup	:	None.
Test Procedure	:	Visually check the connector gender. Measure the dimensions against IEC 807-2 [5].
Conformance	:	A 15-pole male connector having the mechanical mateability dimensions as specified in IEC 807-2 shall be used for the line interface connector.

Test Case ID	:	1411.19.02
Test Case Name	:	AUI connector locking posts and mounting.
Status	:	CONDITIONAL (Only tested if the AUI is implemented and available for testing).
Standard Reference	:	7.6.1
PICS Reference	:	14.10.4.6.6/5
History	:	
Test Purpose	:	To verify the existence and dimensions of the AUI connector locking mechanism.
Note	:	
Test Setup	:	None.
Test Procedure	:	Visually check the connector for the presence of locking posts. Measure the locking post dimensions against Fig 7-18. Verify the connector mounting against Fig 7-20.
Conformance	:	All female connectors shall have the slide latch, and all male connectors shall have the locking posts (as defined in Figs 7-18, 7-19, and 7-20) as the retention system.

Test Case ID	:	1411.19.03
Test Case Name	:	AUI connector pin occupancy.
Status	:	CONDITIONAL (Only tested if the AUI is implemented and available for testing).
Standard Reference	:	7.6.3
PICS Reference	:	14.10.4.6.6/6-21
History	:	
Test Purpose	:	To verify the existence of the AUI connector pins for the AUI circuits.
Note	:	
Test Setup	:	None.
Test Procedure	:	Visually check the AUI connector on the MAU for the presence of connector pins at positions 1, 2, 3, 4, 5, 6, 9, 10, 11, 12, 13 and

		14.
Conformance	:	All pins are present for circuits and shields as defined by the PICS.

Test Case ID	:	1411.19.04
Test Case Name	:	AUI connector shield life.
Status	:	CONDITIONAL (Only tested if the AUI is implemented and available for testing).
Standard Reference	:	7.6.2
PICS Reference	:	14.10.4.6.6/2, 14.10.4.6.6/4
History	:	
Test Purpose	:	To verify the AUI connector shield life.
Note	:	Since this test may be destructive, it is recommended that it be performed last.
Test Setup	:	None.
Test Procedure	:	Using a female AUI connector, mate and unmate to the AUI connector on the MAU for a minimum of 500 cycles. Measure the resistance between the male front shell and the female connector shell.
Conformance	:	The resistance of the cable shield to equipment chassis shall not exceed 5 mΩ, after a minimum of 500 cycles of mating and unmating.

6.3 Test Setups, Signals and Adapters Description. This section describes the test setups, test signals, adapters and instruments used in the abstract test suite.

6.3.1 Test Signal Definitions. Unless otherwise stated, all AUI-DO signals shall have a 56 bit preamble as defined in section 4.2.5 [3] and Start Frame Delimiter (SFD) preceding the test pattern and a start of idle (SOI) following the test pattern with nominal AUI amplitude (1V peak) and edge transition times (0.2 V/ns) into a 78 Ω resistive load. In addition, unless otherwise stated, all MAU-RD signals are defined across a 100 Ω resistive load when driven from a 100 Ω source impedance, have a peak amplitude of 585 mV, and a tolerance on pulse widths of ±1 ns. A cross reference table listing test signals and test cases is shown in A1.2.

Signal Number	Signal Description
1	An AUI-DO signal consisting of a single frame of 512 bits of pseudo-random data.
2a	An AUI-DO signal consisting of repeating frames of 512 bits of pseudo-random data separated by a 4.7 µs inter-packet gap with a peak amplitude of 375 mV.
2b	An AUI-DO signal consisting of repeating frames of 512 bits of pseudo-random data separated by a 4.7 µs inter-packet gap with a peak amplitude of 565 mV.
2c	An AUI-DO signal consisting of repeating frames of 512 bits of pseudo-random data separated by a 4.7 µs inter-packet gap with a peak amplitude of 750 mV.
2d	An AUI-DO signal consisting of repeating frames of 512 bits of pseudo-random data separated by a 4.7 µs inter-packet gap with a peak amplitude of 940 mV.
2e	An AUI-DO signal consisting of repeating frames of 512 bits of pseudo-random data separated by a 4.7 µs inter-packet gap with a peak amplitude of 1130 mV.

2f	An AUI-DO signal consisting of repeating frames of 512 bits of pseudo-random data separated by a 4.7 µs inter-packet gap with a peak amplitude of 1315 mV.
3a	A continuous 5 MHz square wave with a peak amplitude of 375 mV.
3b	A continuous 10 MHz square wave with a peak amplitude of 375 mV.
4	An AUI-DO signal consisting of repeating frames of 1518 bytes of alternating 1's and 0's with a 9.6 µs inter-packet gap.
5	An AUI-DO signal consisting of repeating sequences of preamble and SFD followed by manchester encoded 1's lasting for 19 ms, followed by a 9.6 µs gap.
6	An AUI-DO signal consisting of a single frame of 1518 bytes of pseudo-random data with a minimum pattern length of 511 bits. Amplitude of 318 mV and maximum edge transition times.
7a	A MAU-RD signal consisting of five pairs of sequences of six alternating polarity pulses with a peak amplitude of 585 mV, when measured at the MDI, with a rising edge described by 585 mV * sin(2 π*t/PW), and a falling edge described by 585 mV * sin(2 π(t-PW/2)/PW), where PW is either 73 or127 ns. The first sequence has a pulse width of 73 ns on the positive polarity and 127 ns on the negative polarity. The second sequence has a pulsewidth of 127 ns on the positive polarity and 73 ns on the negative polarity. These five pairs of sequences are followed by a continuous series of repeating pair of sequences of six alternating polarity one-half cycle sine-wave pulses with a peak amplitude of 585 mV when measured at the MDI. The first sequence has a pulse width of 23 ns (+1,-0 ns) on the positive polarity and 77 ns on the negative polarity. The second sequence has a pulse width of 77 ns on the positive polarity and 23 ns (+1,-0 ns) on the negative polarity (see Fig 6-3 and Fig 14-16 [6]). [Note: this signal is equivalent to 60 cycles of a maximally jittered 5 MHz signal (30 cycles of maximum jitter in each direction) followed by a maximally jittered 10 MHz signal, all at minimum amplitude.]
7b	A MAU-RD signal consisting of five pairs of sequences of six alternating polarity pulses with a peak amplitude of 585 mV, when measured at the MDI, with a rising edge described by 585 mV * sin(2 π*t/PW), and a falling edge described by 585 mV * sin(2 π(t-PW/2)/PW), where PW is either 73 or 127 ns. The first sequence has a pulse width of 127 ns on the positive polarity and 73 ns on the negative polarity. The second sequence has a pulsewidth of 73 ns on the positive polarity and 127 ns on the negative polarity. These five pairs of sequences are followed by a continuous series of repeating pair of sequences of six alternating polarity one-half cycle sine-wave pulses with a peak amplitude of 585 mV when measured at the MDI. The first sequence has a pulse width of 77 ns on the positive polarity and 23 ns (+1,-0 ns) on the negative polarity. The second sequence has a pulse width of 23 ns (+1,-0 ns) on the positive polarity and 77 ns on the negative polarity (see Fig 6-3 and Fig 14-16 [6]). [Note: this signal is equivalent to 60 cycles of a maximally jittered 5 MHz signal (30 cycles of maximum jitter in each direction) followed by a maximally jittered 10 MHz signal, all at minimum amplitude.]

8a	A MAU-RD signal consisting of a repeating pair of sequences of five alternating polarity trapezoidal pulses with a peak amplitude of 3.1 V, when measured at the MDI, and a rise and fall slope of 0.5 V/ns. The first sequence has a pulse width of 23 ns (+1,-0 ns) on the positive polarity and 77 ns on the negative polarity. The second sequence has a pulsewidth of 77 ns on the positive polarity and 23 ns (+1,-0 ns) on the negative polarity (see Fig 6-4 and Fig 14-16 [6]).
8b	A MAU-RD signal consisting of a continuous series of repeating pair of sequences of five alternating polarity trapezoidal pulses with a peak amplitude of 3.1 V, when measured at the MDI, and a rise and fall slope of 0.5 V/ns. The first sequence has a pulse width of 77 ns on the positive polarity and 23 ns (+1,-0 ns) on the negative polarity. The second sequence has a pulsewidth of 23 ns (+1,-0 ns) on the positive polarity and 77 ns on the negative polarity (see Fig 6-4 and Fig 14-16 [6]).
9	A MAU-RD signal consisting of a continuous 10 MHz sine-wave with a peak amplitude of 585 mV.
10	A MAU-RD signal consisting of a continuous series of repeating pair of sequences of five alternating polarity trapezoidal pulses with a peak amplitude of 3.1 V, when measured at the MDI, and a rise and fall slope of 0.5 V/ns. The first sequence has a pulse width of 127 ns on the positive polarity and 70 ns on the negative polarity. The second sequence has a pulsewidth of 70 ns on the positive polarity and 127 ns on the negative polarity (see Fig 6-5 and Fig 14-17 [6]).
11a	A MAU-RD signal consisting of a continuous 1 MHz sine-wave with a peak amplitude of 299 mV when measured across a 121 Ω resistive load.
11b	A MAU-RD signal consisting of a continuous 5 MHz sine-wave with a peak amplitude of 299 mV when measured across a 121 Ω resistive load.
11c	A MAU-RD signal consisting of a continuous 10 MHz sine-wave with a peak amplitude of 312 mV when measured across a 121 Ω resistive load.
11d	A MAU-RD signal consisting of a continuous 15 MHz sine-wave with a peak amplitude of 423 mV when measured across a 121 Ω resistive load.
11e	A MAU-RD signal consisting of a continuous 20 MHz sine-wave with a peak amplitude of 769 mV when measured across a 121 Ω resistive load.
11f	A MAU-RD signal consisting of a continuous 25 MHz sine-wave with a peak amplitude of 1.416 V when measured across a 121 Ω resistive load.
11g	A MAU-RD signal consisting of a continuous 30 MHz sine-wave with a peak amplitude of 2.41 1 V when measured across a 121 Ω resistive load.
12a	A MAU-RD signal consisting of a continuous 0.5 MHz sine-wave with a peak-to-peak amplitude of 6.1 V.
12b	A MAU-RD signal consisting of a continuous 1 MHz sine-wave with a peak-to-peak amplitude of 6.1 V.
12c	A MAU-RD signal consisting of a continuous 1.9 MHz sine-wave with a peak-to-peak amplitude of 6.1 V.

13a	A MAU-RD signal consisting of a single cycle 2 MHz sine-wave with a peak-to-peak amplitude of 6.1 V preceded and followed by 4 BT of silence.
13b	A MAU-RD signal consisting of a single cycle 5 MHz sine-wave with a peak-to-peak amplitude of 6.1 V preceded and followed by 4 BT of silence.
13c	A MAU-RD signal consisting of a single cycle 10 MHz sine-wave with a peak-to-peak amplitude of 6.1 V preceded and followed by 4 BT of silence.
13d	A MAU-RD signal consisting of a single cycle 15 MHz sine-wave with a peak-to-peak amplitude of 6.1 V preceded and followed by 4 BT of silence.
14	A MAU-RD signal consisting of a single packet of 512 bits of pseudo-random data, with only 2.3 BT of SOI following the data, followed by a continuous 10 MHz sine-wave with a peak amplitude of 312 mV starting at a phase angle of 180 degrees (i.e. test signal 11c starting in the negative going direction) (see Fig 6-6).
15	A MAU-RD signal consisting of a single frame of 512 bits of pseudo-random data. Amplitude of 585 mV peak and maximum edge transition times.
16	A MAU-RD signal consisting of repeating frames of 512 bits of pseudo-random data. Amplitude of 585 mV peak, maximum edge transition times and an inter-packet gap of 9.6 µs.
17	A 25 V peak-to-peak squarewave with maximum frequency of 500 kHz and with edges no slower than 4 ns (20-80%).
18	An AUI-DO signal consisting of a single packet of 512 bits of pseudo-random data, repeating every 1 ms for a total signal duration of 151 ms.
19a	An AUI-DO signal consisting of a single frame of 512 bits of manchester encoded 1's.
19b	An AUI-DO signal consisting of a single frame of 512 bits of manchester encoded alternating 1's and 0's.
20	An AUI-DO signal consisting of a single frame of 512 bits of pseudo-random data. Amplitude of 159 mV peak and maximum edge transition times.
21a	A continuous 30 Hz sine-wave with a peak amplitude of 3.0 V.
21b	A continuous 20 kHz sine-wave with a peak amplitude of 3.0 V.
21c	A continuous 40 kHz sine-wave with a peak amplitude of 3.0 V.
21d	A continuous 500 kHz sine-wave with a peak amplitude of 200 mV.
21e	A continuous 1 MHz sine-wave with a peak amplitude of 200 mV.
21f	A continuous 5 MHz sine-wave with a peak amplitude of 200 mV.
21g	A continuous 10 MHz sine-wave with a peak amplitude of 200 mV.
22a	A continuous 30 Hz sine-wave with a peak amplitude of 3.0 V AC and a DC offset of 2.5V.
22b	A continuous 20 kHz sine-wave with a peak amplitude of 3.0 V AC and a DC offset of 2.5V.
22c	A continuous 40 kHz sine-wave with a peak amplitude of 3.0 V AC and a DC offset of 2.5V.
22d	A continuous 30 Hz sine-wave with a peak amplitude of 3.0 V AC and a DC offset of -2.5V.

22e	A continuous 20 kHz sine-wave with a peak amplitude of 3.0 V AC and a DC offset of -2.5V.
22f	A continuous 40 kHz sine-wave with a peak amplitude of 3.0 V AC and a DC offset of -2.5V.
22g	A continuous 500 kHz sine-wave with a peak amplitude of 200 mV AC and a DC offset of 5.3 V.
22h	A continuous 1 MHz sine-wave with a peak amplitude of 200 mV AC and a DC offset of 5.3 V.
22i	A continuous 5 MHz sine-wave with a peak amplitude of 200 mV AC and a DC offset of 5.3 V.
22j	A continuous 10 MHz sine-wave with a peak amplitude of 200 mV AC and a DC offset of 5.3 V.
22k	A continuous 500 kHz sine-wave with a peak amplitude of 200 mV AC and a DC offset of -5.3 V.
22l	A continuous 1 MHz sine-wave with a peak amplitude of 200 mV AC and a DC offset of -5.3 V.
22m	A continuous 5 MHz sine-wave with a peak amplitude of 200 mV AC and a DC offset of -5.3 V.
22n	A continuous 10 MHz sine-wave with a peak amplitude of 200 mV AC and a DC offset of -5.3 V.
23a	An AUI-DO signal consisting of a single frame of 512 bits of manchester encoded 1's, with the signal remaining HI for 1.6 BT after the last low to high transition (see Fig 6-7). Amplitude of 375 mV peak.
23b	An AUI-DO signal consisting of a single frame of 512 bits of manchester encoded 1's, with the signal remaining HI for 1.6 BT after the last low to high transition (see Fig 6-7). Amplitude of 1170 mV peak.
24a	An AUI-DO signal consisting of repeating frames of 512 bits of pseudo-random data separated by a 4.7 µs inter-packet gap with a peak amplitude of 585 mV.
24b	An AUI-DO signal consisting of repeating frames of 512 bits of pseudo-random data separated by a 4.7 µs inter-packet gap with a peak amplitude of 1.0 V.
24c	An AUI-DO signal consisting of repeating frames of 512 bits of pseudo-random data separated by a 4.7 µs inter-packet gap with a peak amplitude of 1.5 V.
24d	An AUI-DO signal consisting of repeating frames of 512 bits of pseudo-random data separated by a 4.7 µs inter-packet gap with a peak amplitude of 2.0 V.
24e	An AUI-DO signal consisting of repeating frames of 512 bits of pseudo-random data separated by a 4.7 µs inter-packet gap -with a peak amplitude of 2.5 V.
24f	An AUI-DO signal consisting of repeating frames of 512 bits of pseudo-random data separated by a 4.7 µs inter-packet gap with a peak amplitude of 3.1 V.
25	An AUI-DO signal consisting of repeating frames of 48 bits of data and an inter-packet gap of 50 µs.
26	An AUI-DO signal consisting of repeating sequences of preamble and SFD followed by manchester encoded 1's lasting 7.5 ms, followed by a 9.6 µs gap.

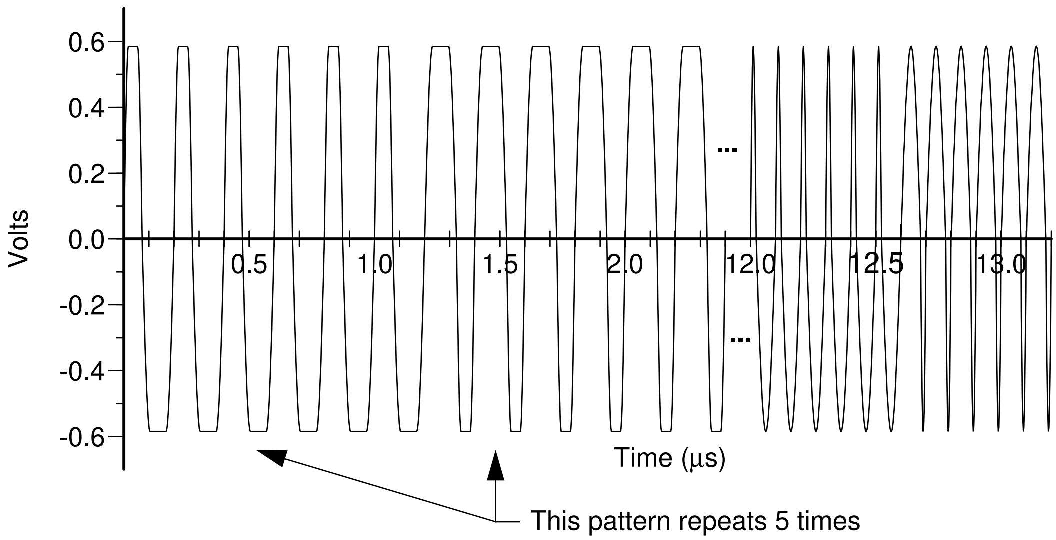


Fig 6-3
Typical Test Signal 7 Waveform

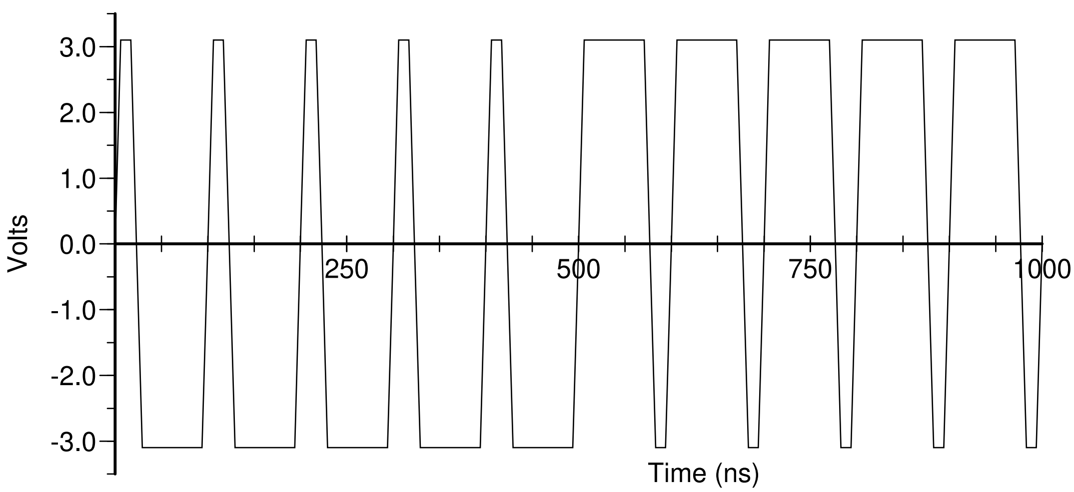


Fig 6-4
Typical Test Signal 8 Waveform

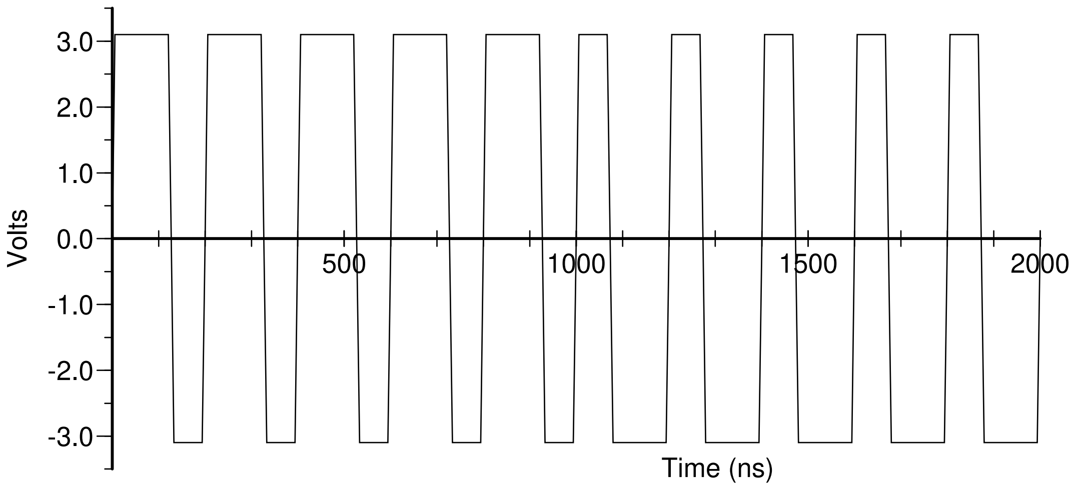


Fig 6-5
Typical T est Signal 10 W aveform

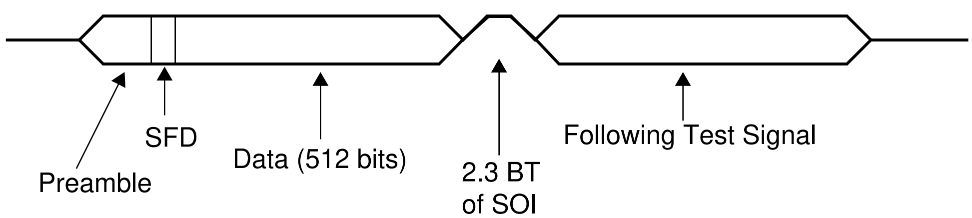


Fig 6-6
Typical T est Signal 14 W aveform

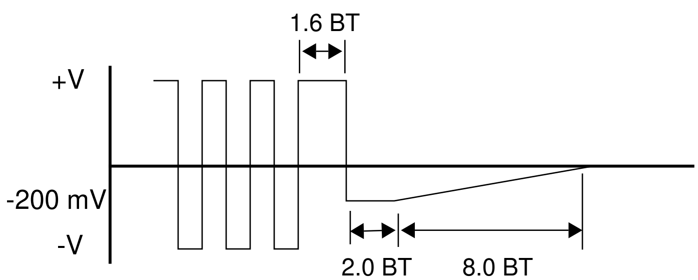


Fig 6-7
Typical T est Signal 23 W aveform

6.3.2 Common T est Setups. Common test setup configurations are referenced in the test cases for the MAU. These are described, in general terms, in Figs 6-8 through 6-38 below . All error terms shall be eliminated or accounted for in the accuracy of the measurement. All load resistors are ±1% unless otherwise noted. In test setups E, F , J, V , AA, BB and EE, the balance of the test equipment (including matching resistors, if any) should exceed that required of the transmitter or receiver (depending on the test). A cross reference table listing test setup identifiers and test cases is shown in A1.3.

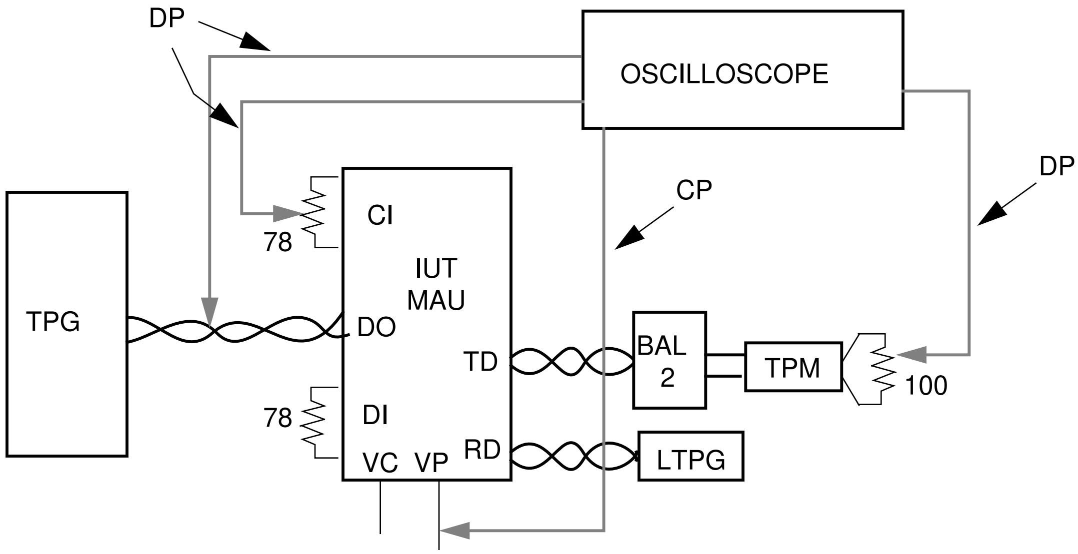


Fig 6-8
Test Setup A

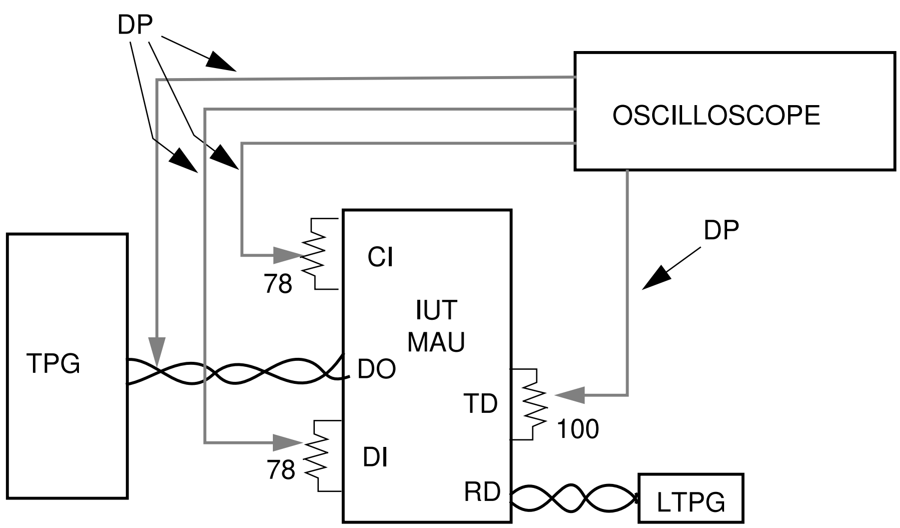


Fig 6-9
Test Setup B

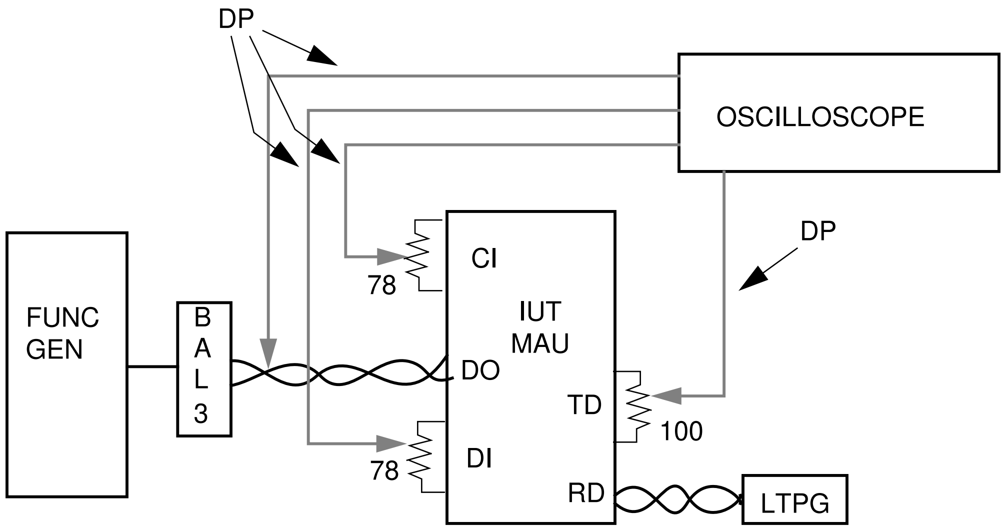


Fig 6-10
Test Setup C

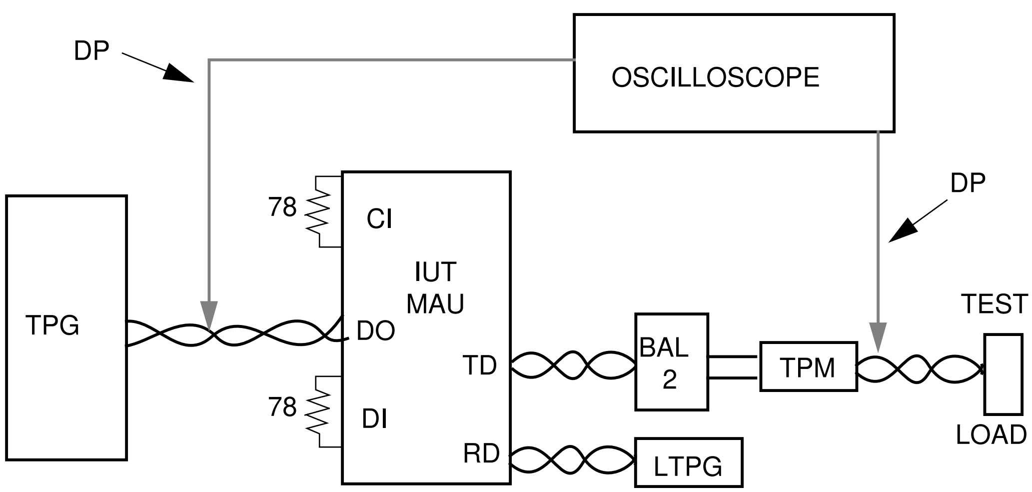


Fig 6-1 1
Test Setup D

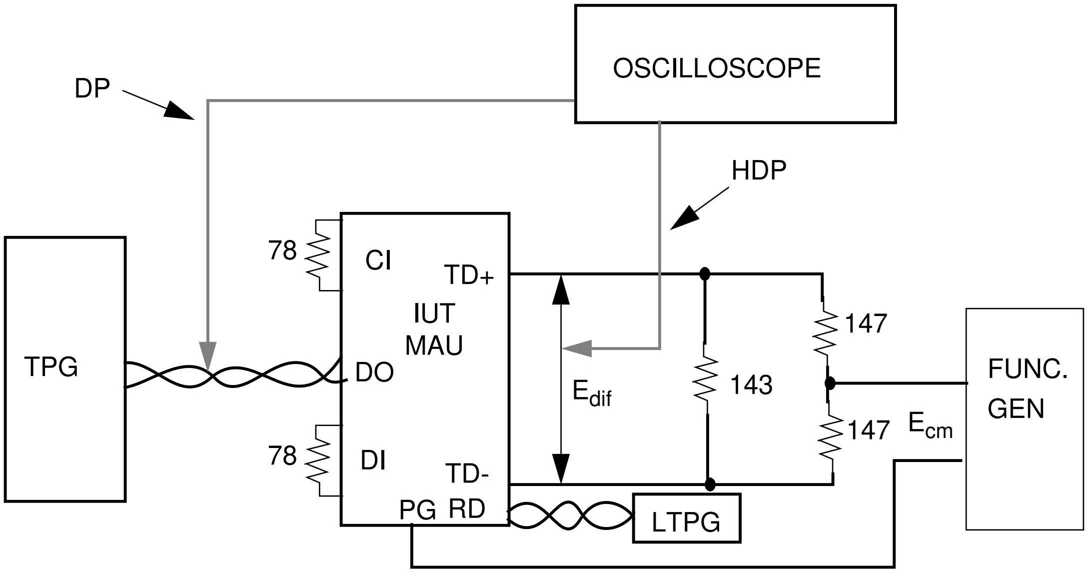


Fig 6-12
Test Setup E

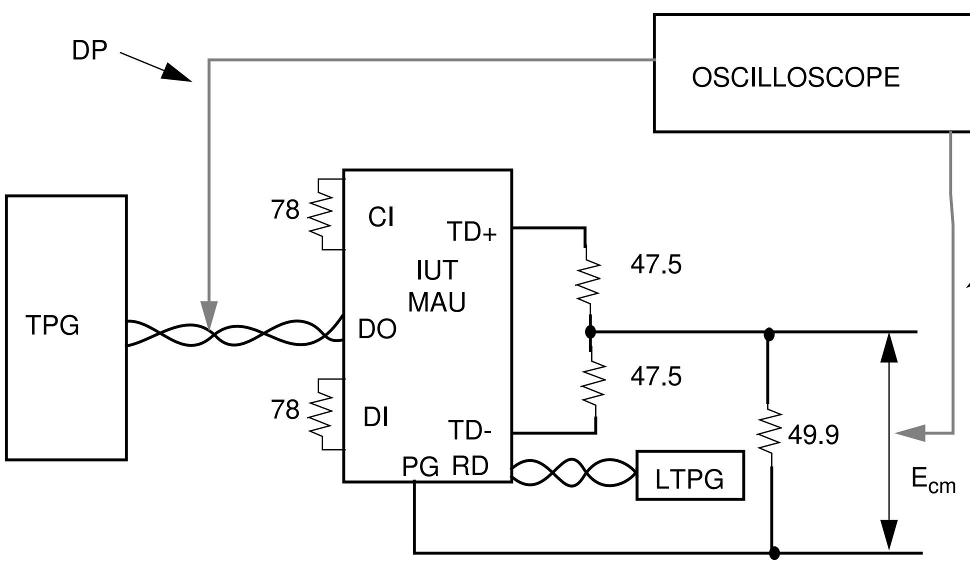


Fig 6-13
Test Setup F

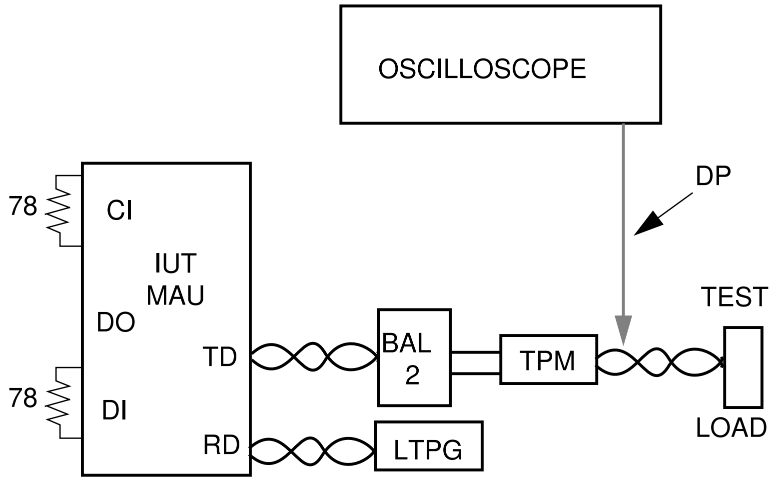


Fig 6-14
Test Setup G

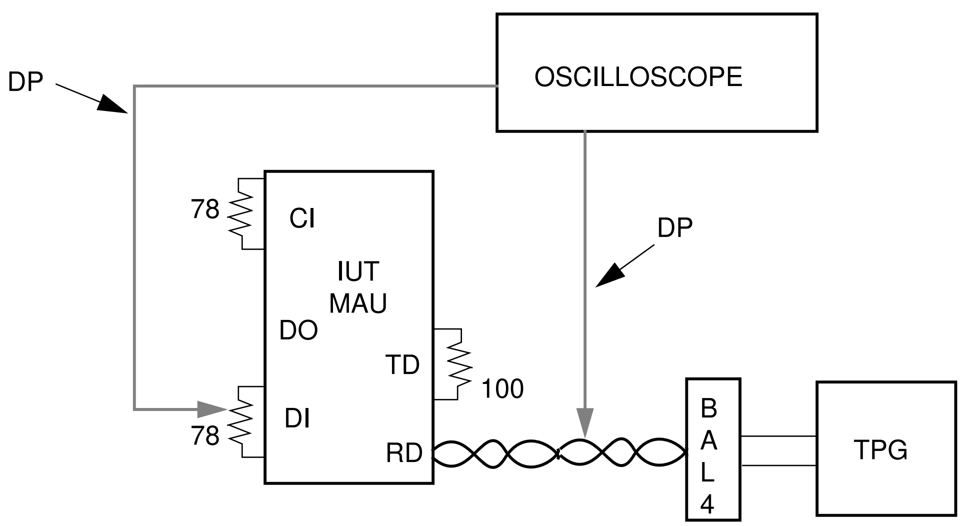


Fig 6-15
Test Setup H

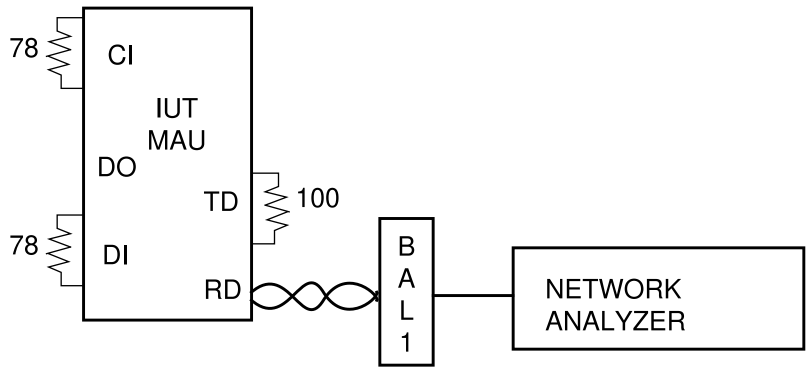


Fig 6-16
Test Setup I

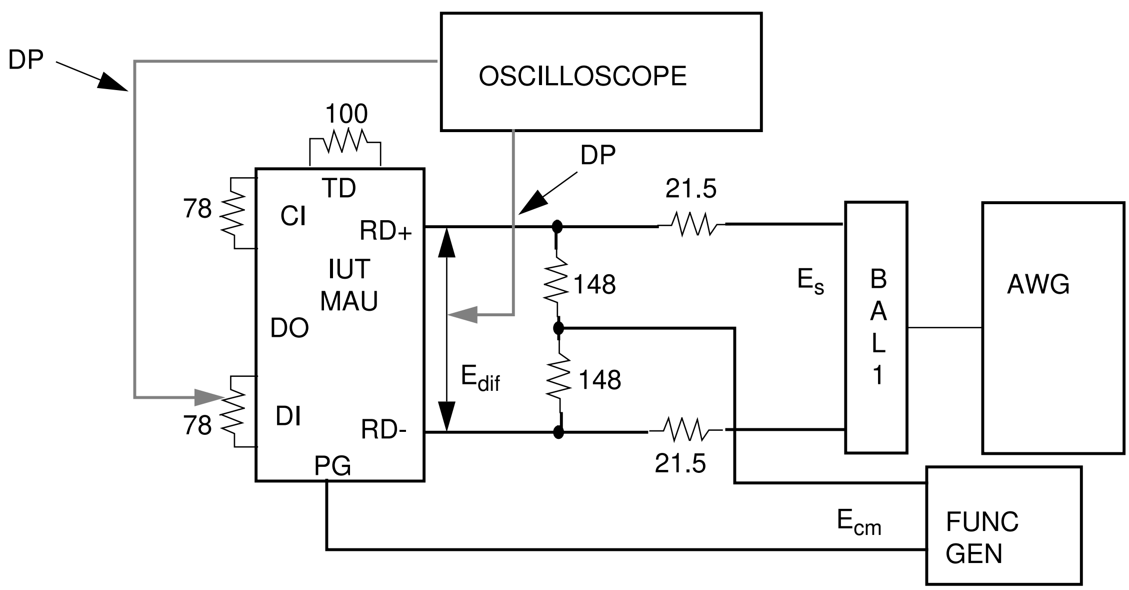


Fig 6-17
Test Setup J

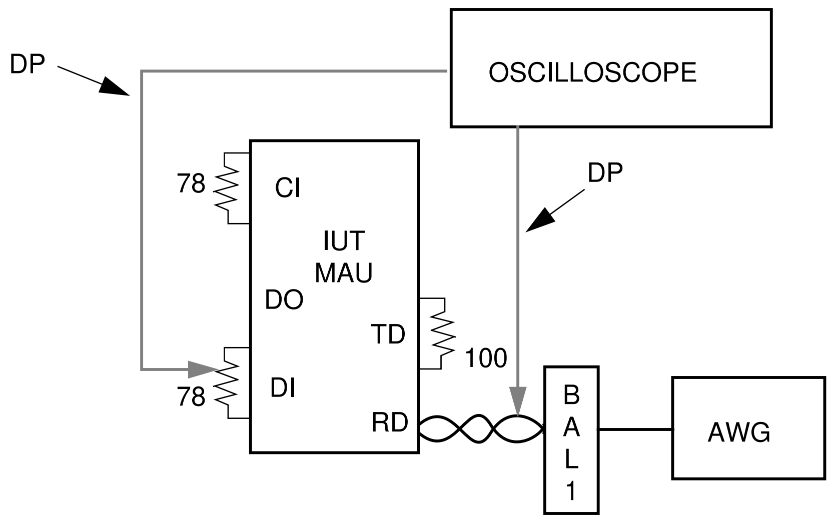


Fig 6-18
Test Setup K

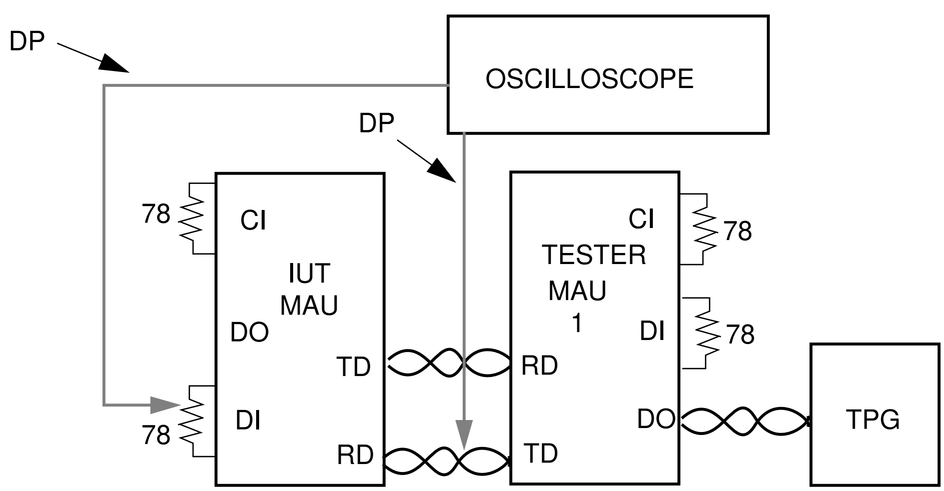


Fig 6-19
Test Setup L

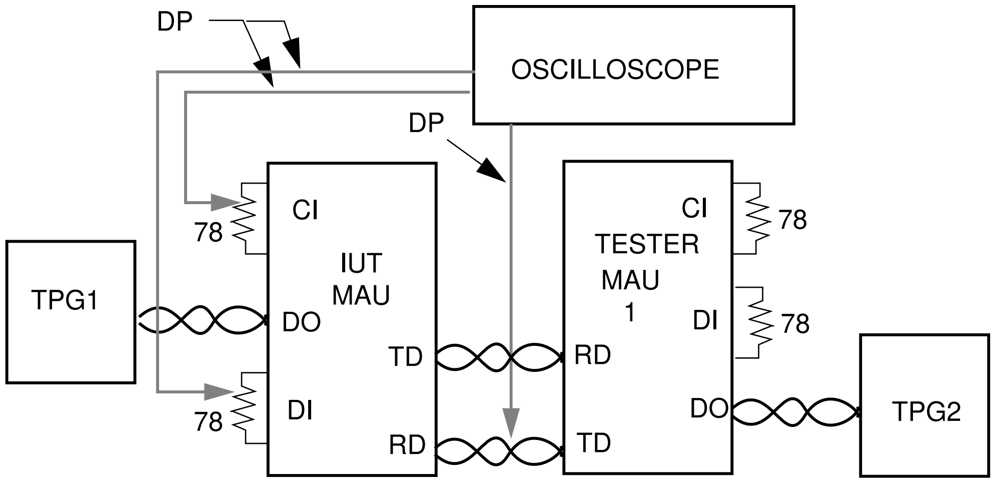


Fig 6-20
Test Setup M

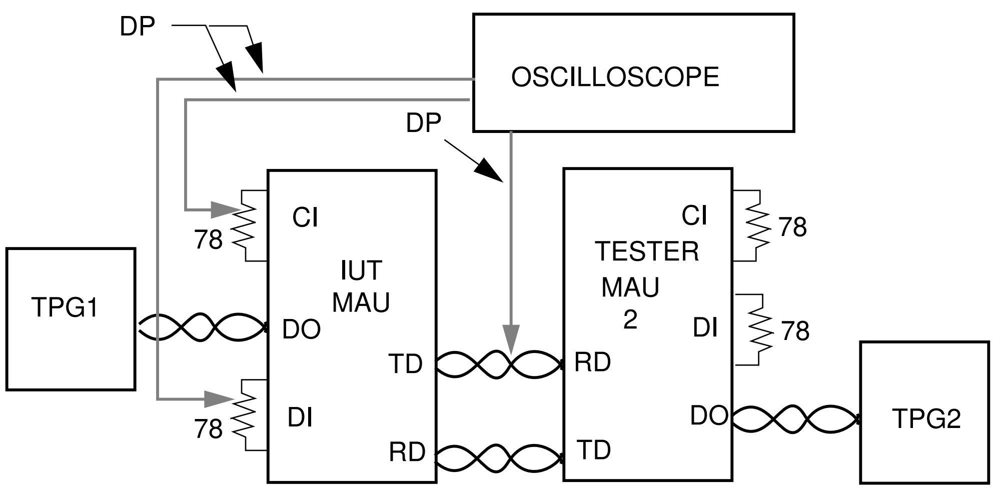


Fig 6-21
Test Setup N

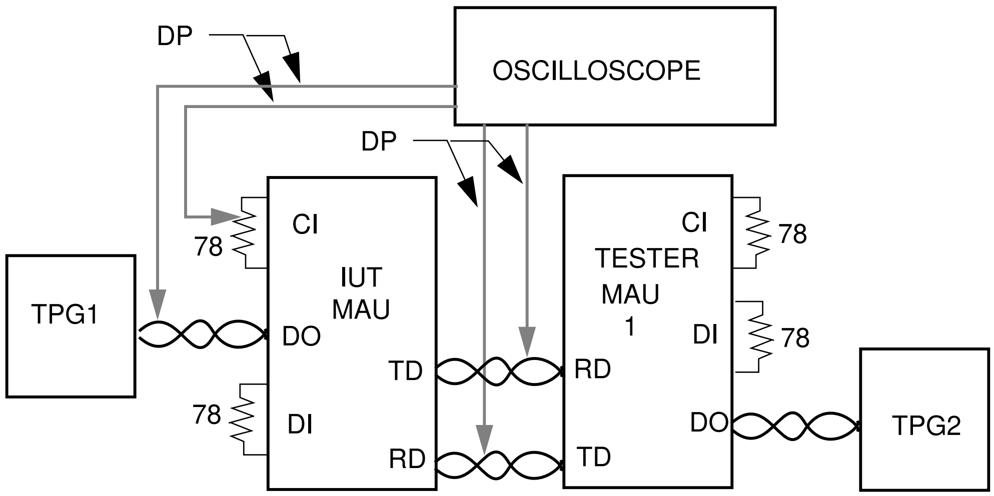


Fig 6-22
Test Setup O

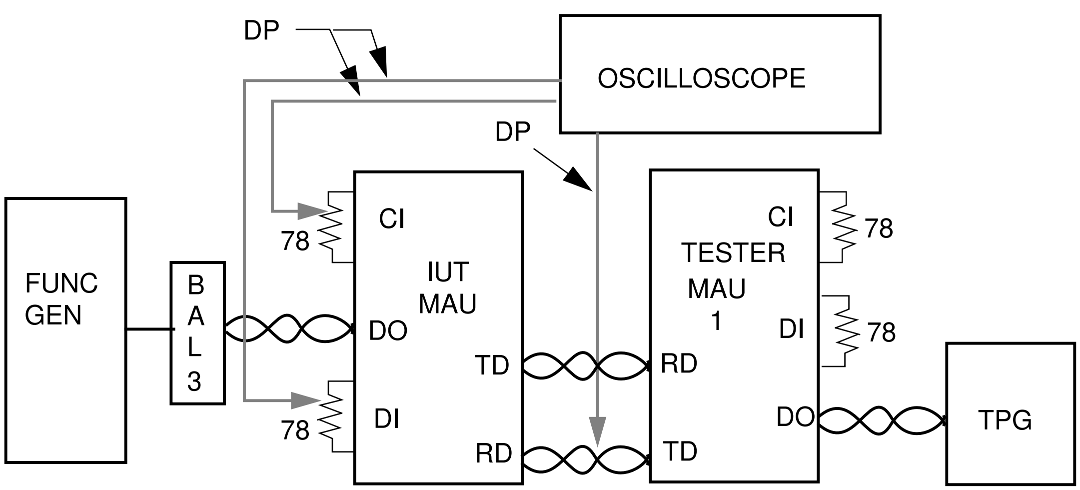


Fig 6-23
Test Setup P

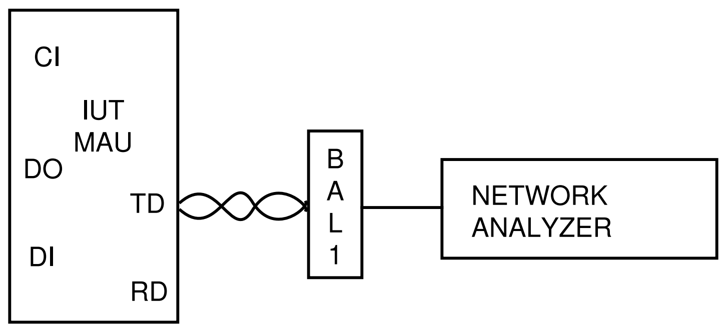


Fig 6-24
Test Setup Q

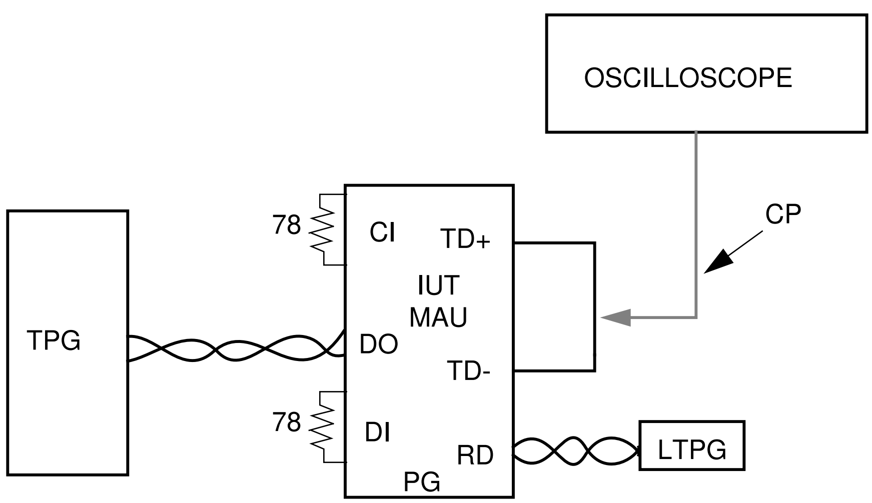


Fig 6-25
Test Setup R

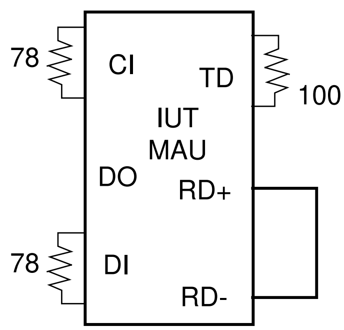


Fig 6-26
Test Setup S

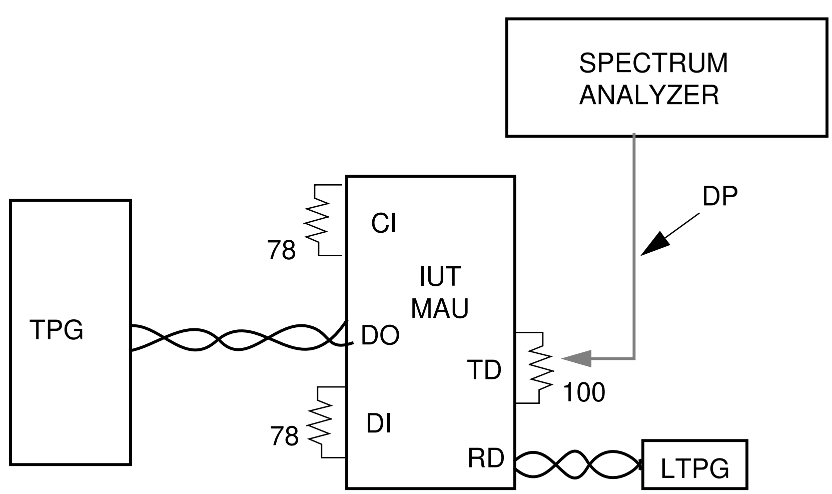


Fig 6-27
Test Setup T

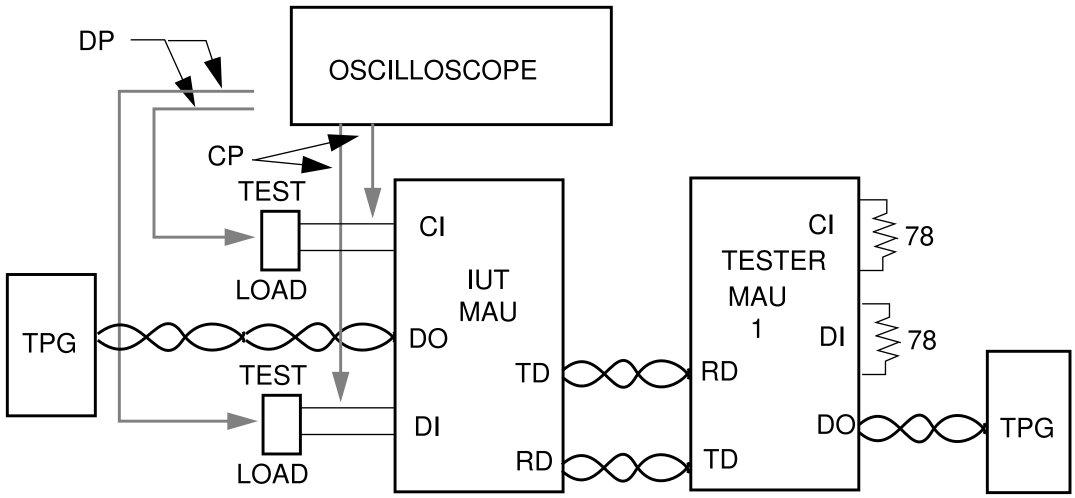


Fig 6-28
Test Setup U

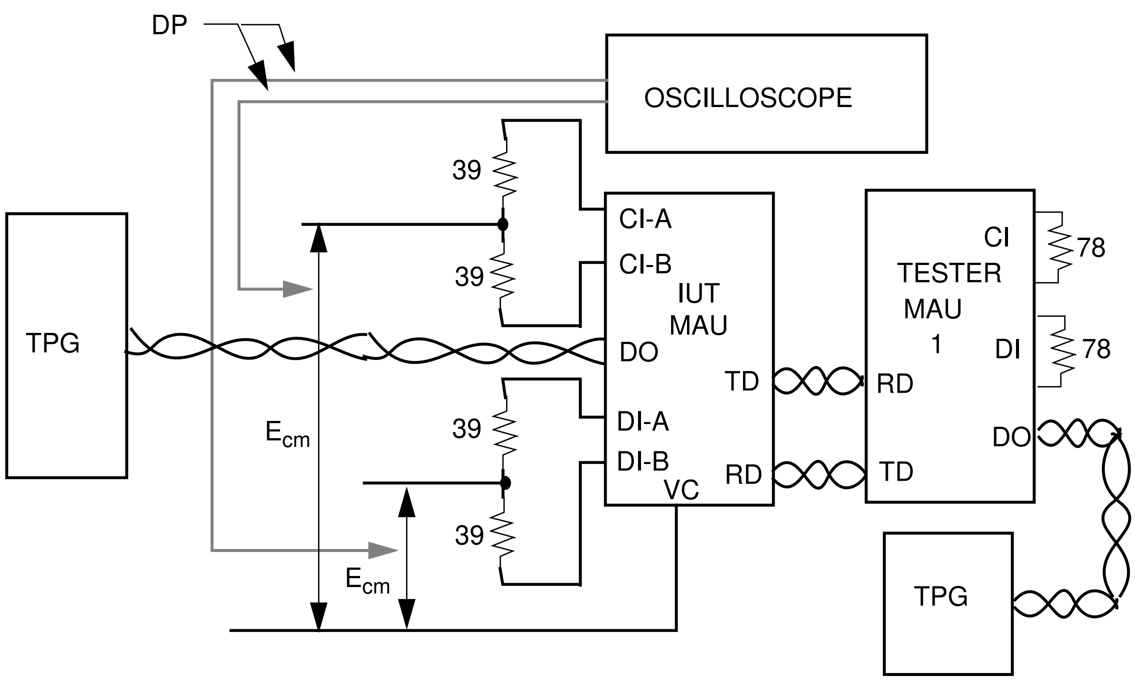


Fig 6-29
Test Setup V

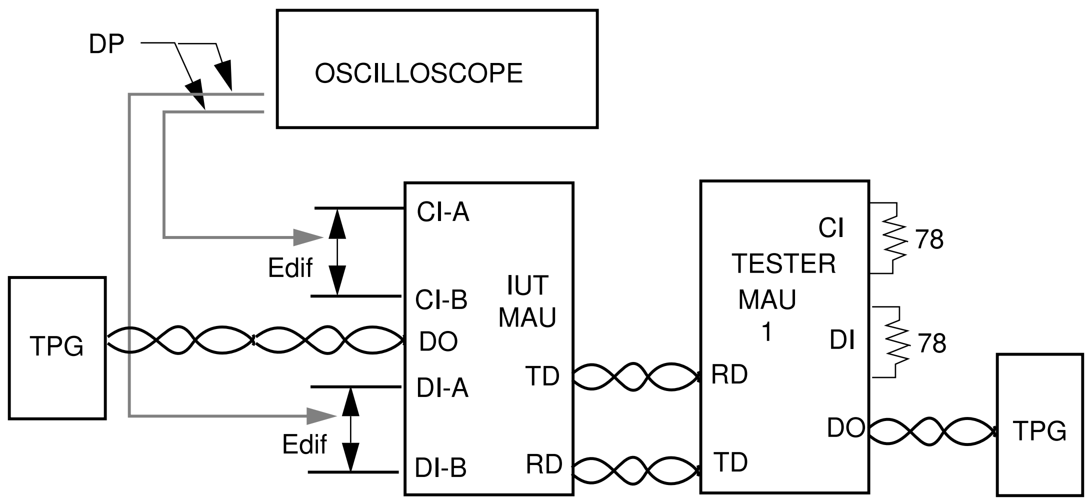


Fig 6-30
Test Setup W

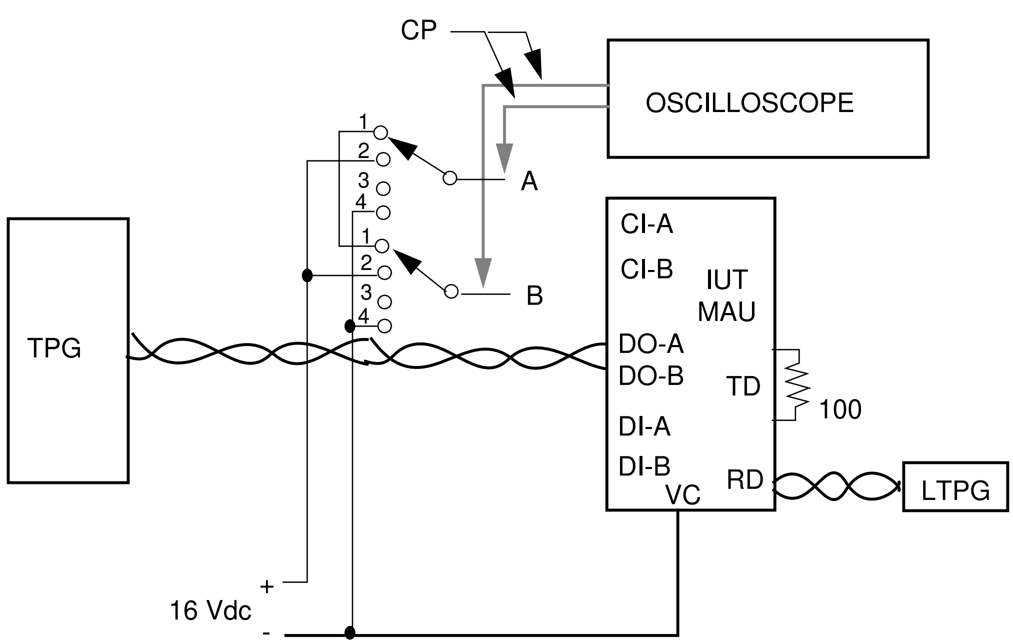


Fig 6-31
Test Setup X

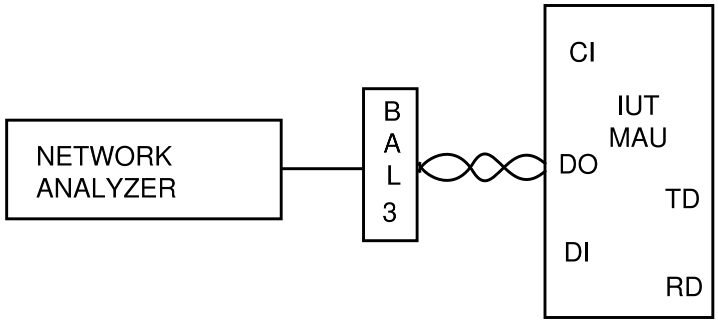


Fig 6-32
Test Setup Y

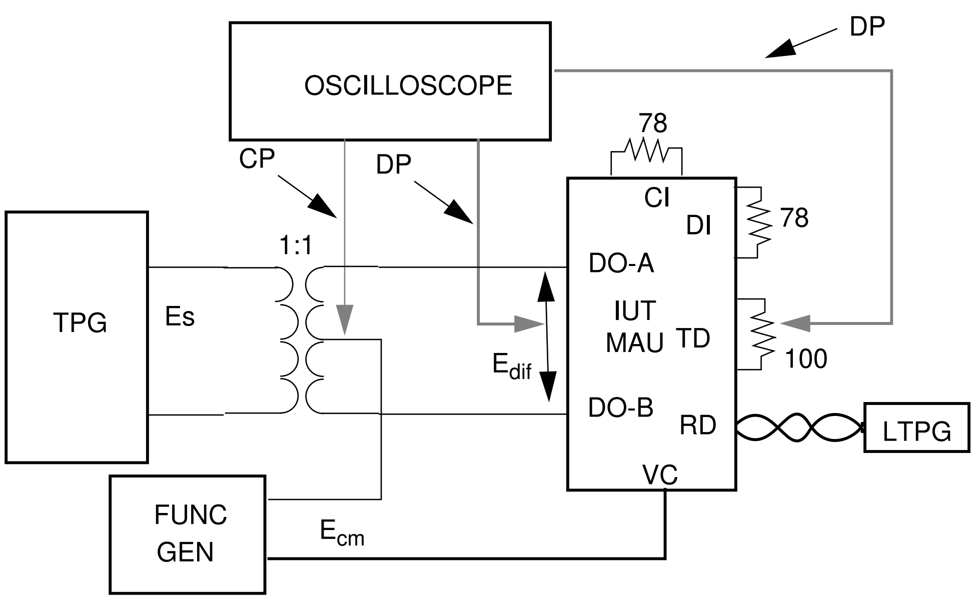


Fig 6-33
Test Setup Z

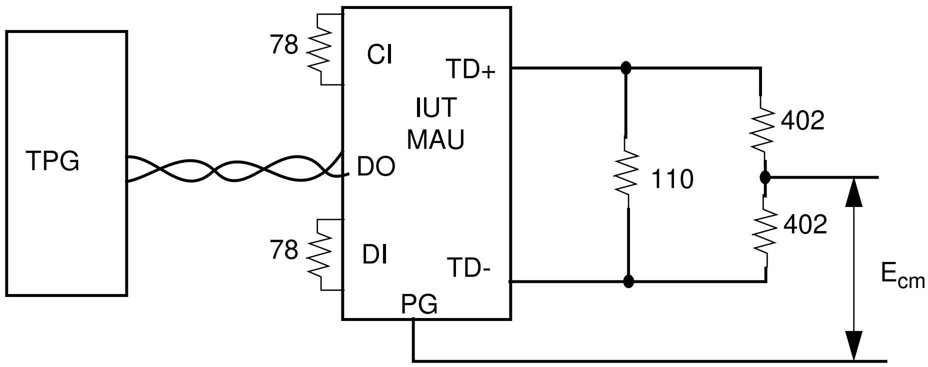


Fig 6-34
Test Setup AA

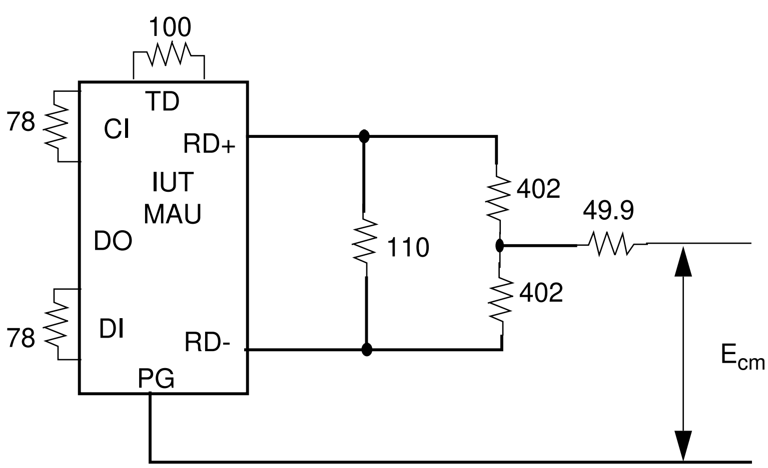


Fig 6-35
Test Setup BB

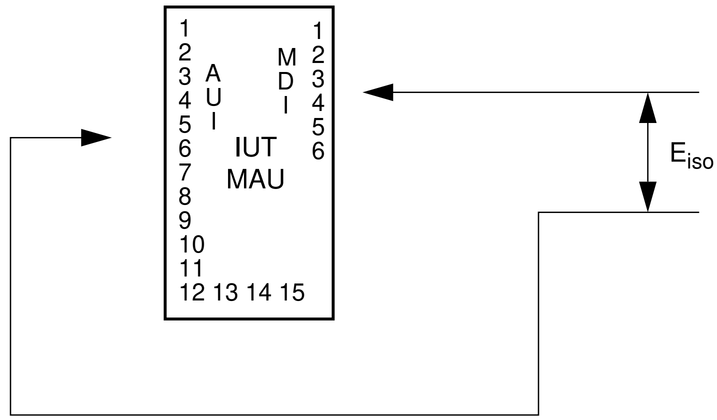


Fig 6-36
Test Setup CC

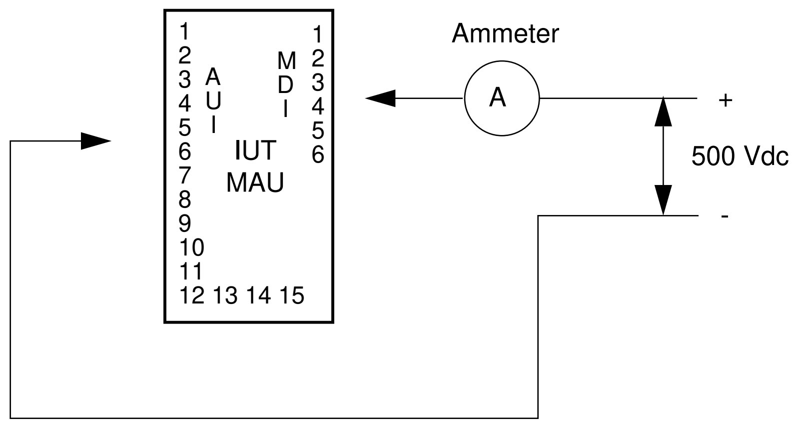


Fig 6-37
Test Setup DD

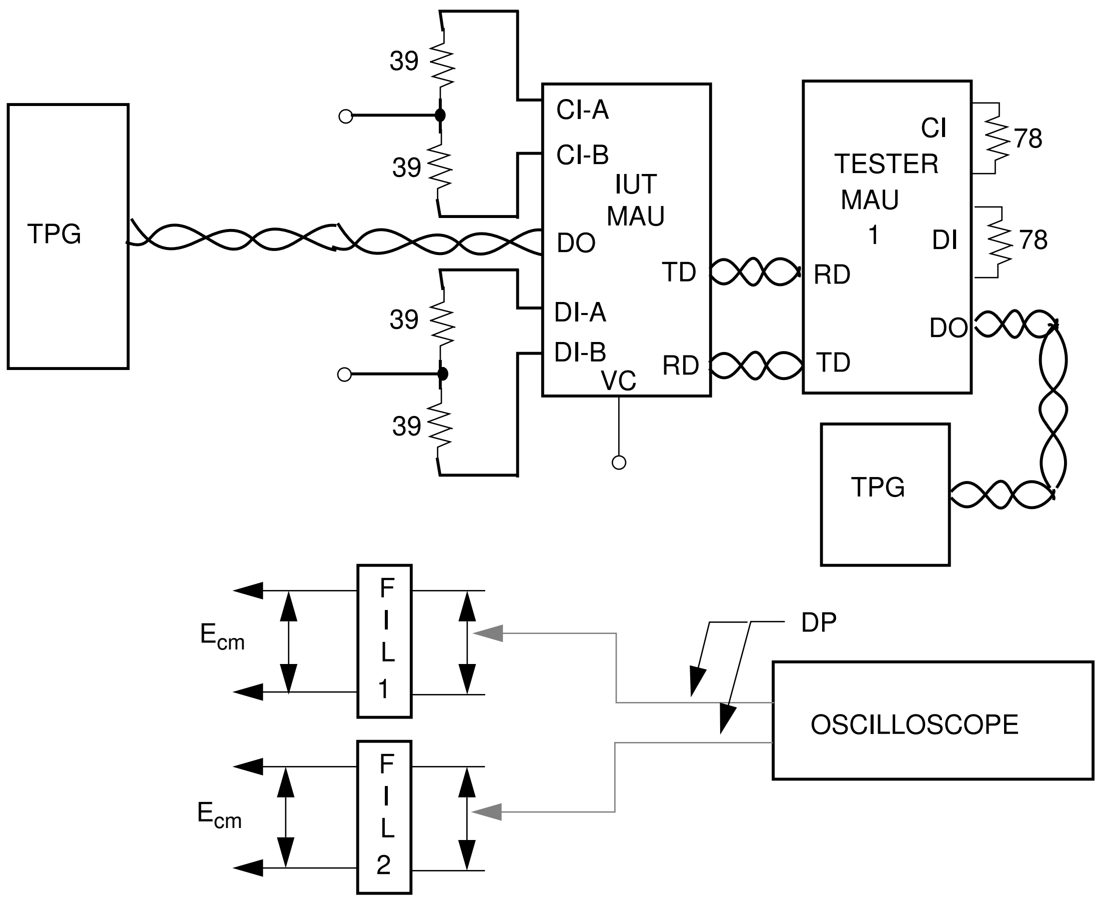


Fig 6-38
Test Setup EE

6.3.3 Special Test Adapters. The test adapters are devices which provide an interface between the test equipment and the MAU under test. The use of these adapters is not mandatory. They are intended to facilitate test implementation. Their exact configuration is dependent on the selected test equipment/instrumentation, the sensitivity of the measurement, cable characteristics and test method. The contribution of impedance mismatch of adapters and terminations shall be taken into account.

6.3.3.1 Test Loads. These are resistive/inductive terminations in accordance with Standard Reference 14.3.1.2.1 (Fig 14-11) [6] and 7.4.1.1 [3].

6.3.3.2 Twisted Pair Model (TPM). This test adapter models the distortion introduced by a link segment. This twisted pair model shall be constructed in accordance with Standard Reference 14.3.1.2 (Fig 14-7) [6].

6.3.3.3 100 Ω to 50 Ω Balun Impedance Adapter (BAL1). This adapter allows a differential signal pair to be properly terminated and matched to a 50 Ω unbalanced impedance. The adapter allows signals on the MAU RD or TD circuits to be monitored or driven by instruments with a 50 Ω impedance. An implementation of the balun may, for example, contain a transformer.

6.3.3.4 100 Ω to 100 Ω TPM Balun (BAL 2). This adapter allows the balanced output of the MAU to be matched to the single-ended Twisted Pair Model (TPM). If the MAU under test has an output transformer embedded internal to the MAU and directly connected to the MDI, then this balun is not required as the embedded transformer will function as the balun.

6.3.3.5 78 Ω to 50 Ω AUI Balun (BAL 3). This adapter allows the balanced MAU DO circuit to be matched to the unbalanced output of the test pattern generator.

6.3.3.6 78 Ω to 100 Ω Balun (BAL4). This adapter allows the unbalanced output of the test pattern generator to be matched to the balanced MAU RD circuit.

6.3.3.7 78 Ω Balanced to Balanced 1:1 Center Tapped Transformer. This allows the application of a common mode signal to the DO circuit of the MAU.

6.3.3.8 Tester MAU 1. This is a conforming MAU.

6.3.3.9 Tester MAU 2. This is a conforming MAU with the generation of link test pulses disabled.

6.3.3.10 30 Hz to 40 kHz Filter (FIL1). This adapter is used in measuring the AC common mode output voltage. It is a bandpass butterworth filter with insertion loss ≤0.5 dB at 20 kHz and input impedance ≥ 1 MΩ. The low pass section shall have Butterworth characteristics consisting of at least 3 poles with a 3 dB cutoff frequency of 40 kHz ± 5%. The high pass section shall have Butterworth characteristics consisting of at least 3 poles with a 3 dB cutoff frequency of 30 Hz ± 5%.

6.3.3.11 40 kHz to BR Filter (FIL2). This adapter is used in measuring the AC common mode output voltage. It is a bandpass butterworth filter with insertion loss ≤0.5 dB at 20 kHz and input impedance ≥ 1 MΩ. The low pass section shall have Butterworth characteristics consisting of at least 3 poles with a 3 dB cutoff frequency of 10 MHz ± 5%. The high pass section shall have Butterworth characteristics consisting of at least 3 poles with a 3 dB cutoff frequency of 40 kHz ± 5%.

6.3.4 Test Equipment Capabilities

(1) All test equipment calibration shall be maintained to the manufacturer's specification.
(2) To satisfy the requirements of MAU testing as specified in section 6.2, the required functionality of the test instruments is given below.
(3) The use of instruments with equivalent functionality is permitted.
(4) The functionality given below is necessary but not sufficient information. The reader should take into account the selected test setup for complete information.

6.3.4.1 Power supply.

Voltage	:	0 - 20 V DC
Current	:	2 A
Load Regulation	:	< 0.01%
Line Stability	:	< 0.01%
Ripple and Noise	:	< 1 mV
Output Impedance (DC)	:	< 5 m Ω
Temp Coeff (0-45 °C)	:	< 0.01%/ °C
Protection AC side	:	Fused
Protection DC side	:	Short circuit and overload

6.3.4.2 Test Pattern Generator (TPG).

Signaling Rate	:	10 Mb/s nominal
Output	:	Balanced pair as per 7.4.1 [3]
Output Impedance	:	78 Ω nominal as per 7.4.1 [3]
Output Jitter	:	< ±0.5 ns to the MAU under test
Output Amplitude	:	Adjustable, ±1.4 V peak
Output Edge Rate	:	5 ns/V
Data Format	:	Manchester encoded serial data.
Signaling	:	Continuous stream or variable length packets with preamble, SFD, n bits of data (pseudo-random, all 1's, alternating 1's and 0's) and start of idle
Repetition Rate	:	Adjustable, single shot to continuous

Note: Media Access Controller (MAC) based implementations of the TPG must not require DO to DI loopback to function properly.

6.3.4.3 Link Test Pulse Generator (LTPG).

Output	:	Balanced pair
Output Impedance	:	100 Ω nominal
Output Amplitude	:	Adjustable
Output Duty Cycle	:	Adjustable
Signaling	:	This is a device that is capable of generating link test pulses in accordance with the transmitter waveform for link test pulses shown in Fig. 14-12 in P802.3i [6].

6.3.4.4 Arbitrary Waveform Generator (AWG).

Output Amplitude	:	±3.1 V
Output Impedance	:	50 Ω
Sample Resolution	:	5 ns/sample
Record Length	:	256K samples, minimum

6.3.4.5 Function Generator (FG).

Output Amplitude	:	0 - 25 V p-p
Output Offset	:	±6 V dc
Output Frequency	:	1 kHz to 21 MHz
Output Impedance	:	50 Ω

6.3.4.6 Spectrum Analyzer.

Frequency coverage	:	1 MHz to 100 MHz
Reference Level Range	:	-70 to +20 dBm
Frequency Response	:	±1.5 dB (1-100 MHz)
Input Impedance	:	50 Ω

6.3.4.7 Network Analyzer.

Frequency Range	:	1 MHz to 100 MHz
Frequency Setting	:	1 Hz
Dynamic Range	:	90 dB
Magnitude Accuracy	:	±0.2 dB
Input Impedance	:	50 Ω
Maximum Drive Level	:	≥ +15 dBm

6.3.4.8 Oscilloscope.

Type	:	Digital Real-Time Sampling or Analog Storage
Trigger	:	Internal and External
Number of Channels	:	4
Samples/Channel	:	20,000 points, min. (applies only to digitizing oscilloscopes)
Bandwidth	:	200 MHz single-shot and repetitive
Timebase	:	2 ns/div to 20 ms/div
Amplitude Accuracy	:	±1 mV
Input Coupling	:	AC, DC; 50 Ω or 1 M Ω
Additional Functions	:	Delayed timebase, waveform math functions (A-B, A+B)

6.3.4.9 Differential Probe/Amplifier (DP).

Bandwidth	:	DC to 100 MHz
CMRR	:	500:1 at 50 MHz
Output Impedance	:	50 Ω or 1 M Ω
Input Impedance	:	1 MΩ

6.3.4.10 High Performance Differential Probe (HDP).

Bandwidth	:	100 kHz to 100 MHz
CMRR	:	1000:1 (60 dB) at 100 MHz
Output Impedance	:	1 MΩ
Input Impedance	:	1 MΩ

6.3.4.1 1 Current Probe/Amplifier (CP).

Bandwidth	:	DC to 50 MHz
Input Current Range	:	1 mA to 10 A DC
Output Impedance	:	50 Ω or 1 M Ω

6.3.4.12 DC Ammeter.

Current Range	:	100 µA to 1 mA DC
Resolution	:	≤ 2 µA

Appendix A (Informative)

Reference Information

(This Appendix is not a part of IEEE Std 1802.3d-199x, but is included for information only.)

A1. 10BASE-T MAU

A1.1 State Diagram Test Coverage. The Figs A1 through A4 show the test cases used to check the different paths through the state diagrams shown in Figs 14-3 through 14-6 [6]. This information is provided as an aid to understanding the state machine test procedures.

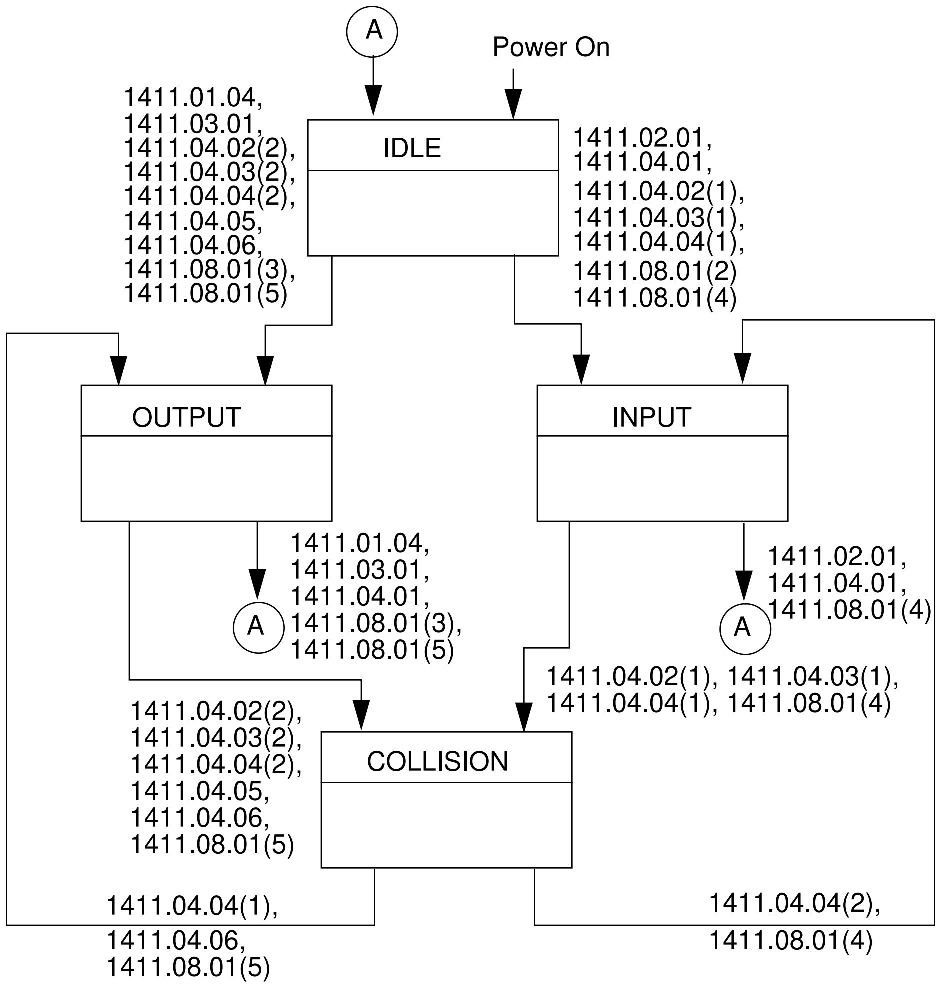


Fig A1
MAU Transmit, Receive, Loopback and Collision Presence Functions State Diagram Coverage

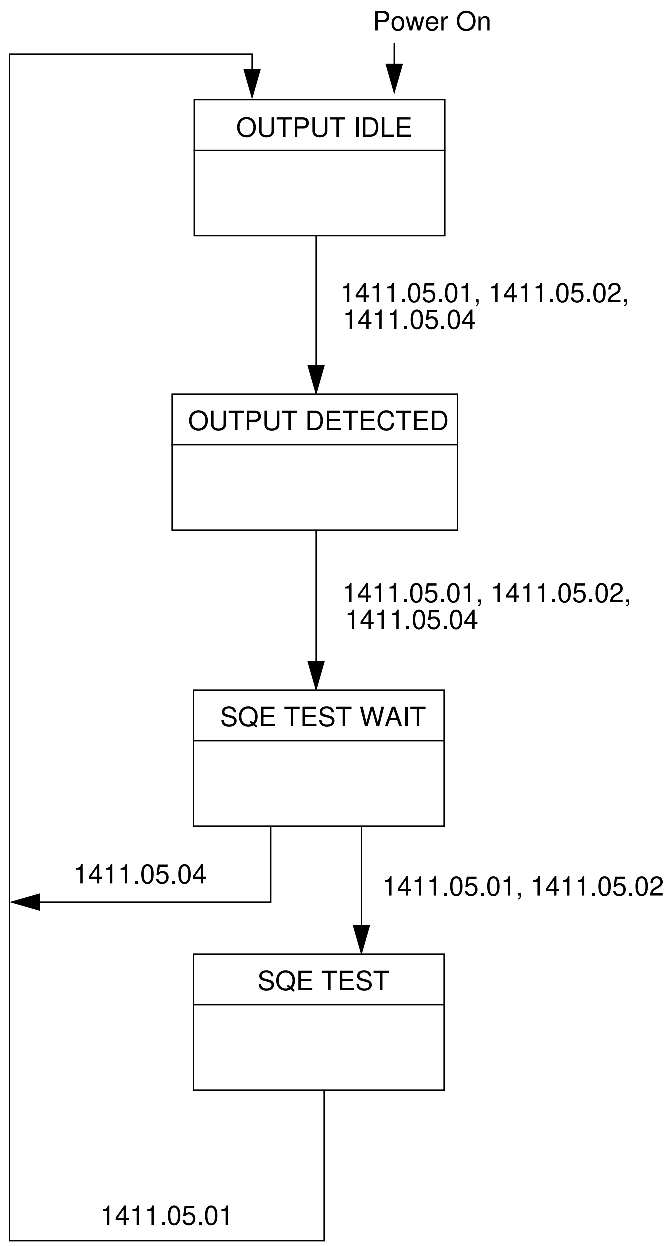


Fig A2
***signal_quality_error* Message**
Test Function State Diagram Coverage

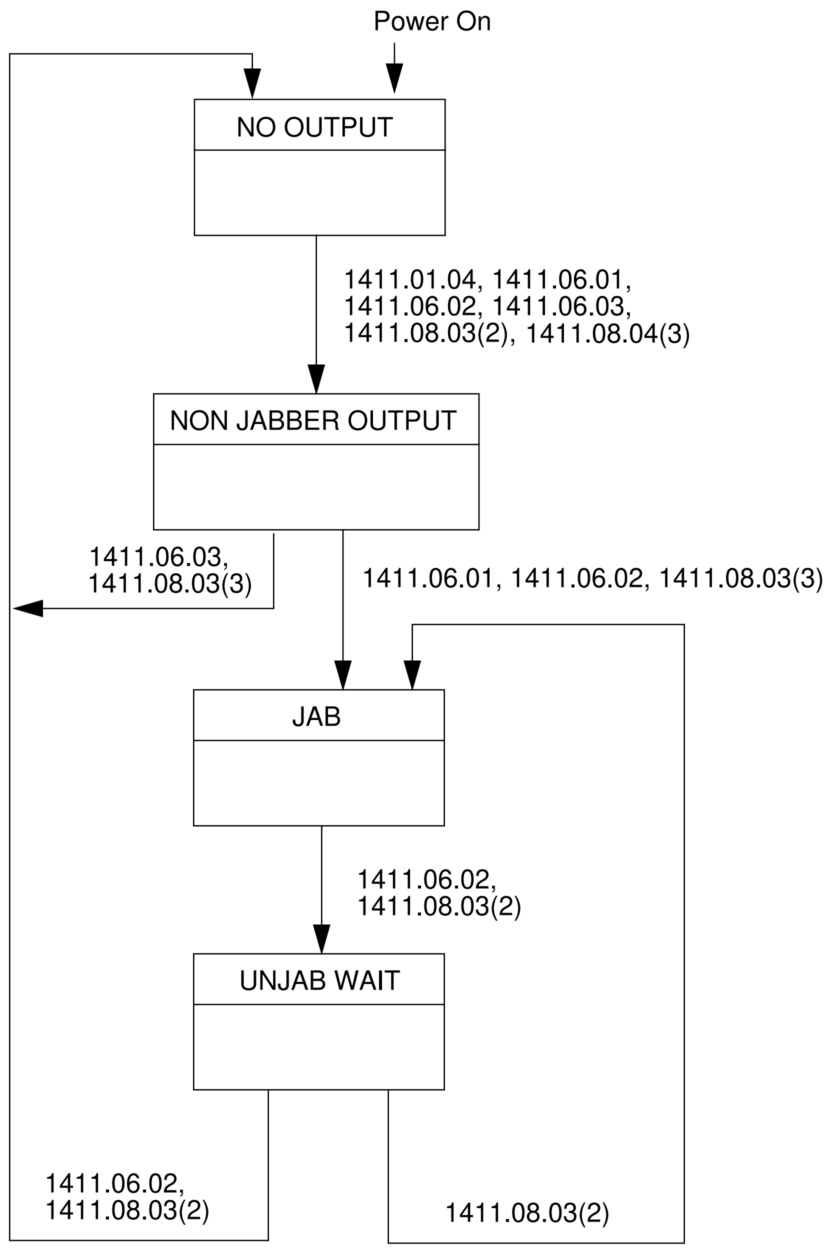


Fig A3
Jabber Function State Diagram Coverage

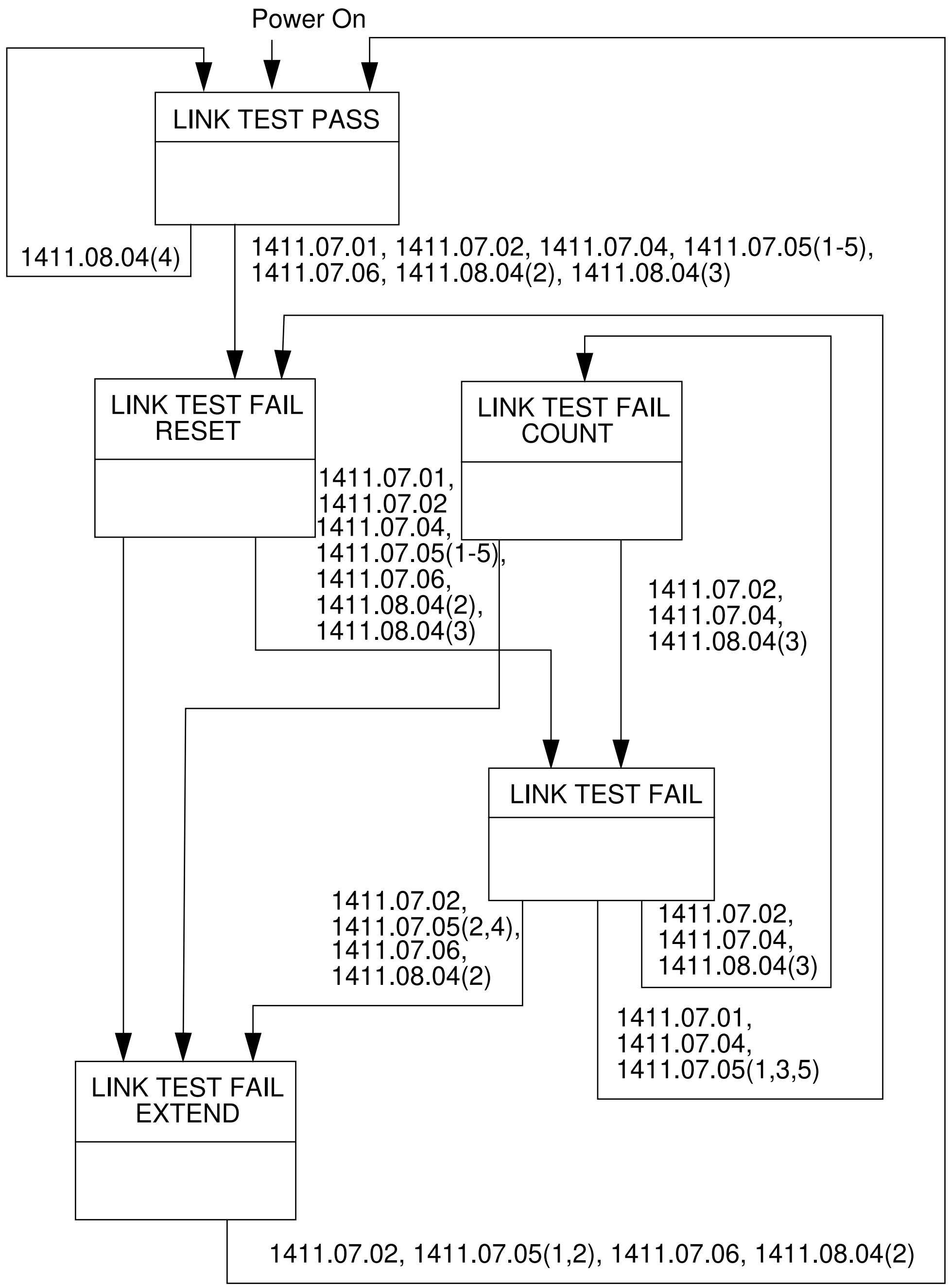


Fig A4
Link Integrity Test Function
State Diagram Coverage

A1.2 Test Signal to Test ID Cross Reference. The following table lists the test cases, by Test ID, that use each of the test signals described in Section 6.3.1.

Test Signal	Test Case(s)
1	141 1.01.01, 141 1.01.02, 141 1.01.03, 141 1.01.04, 141 1.01.06, 141 1.01.07, 141 1.02.01, 141 1.02.02, 141 1.02.03, 141 1.02.05, 141 1.03.01, 141 1.03.02, 141 1.03.03, 141 1.03.04, 141 1.04.01, 141 1.04.02, 141 1.04.03, 141 1.04.04, 141 1.05.01, 141 1.05.02, 141 1.05.03, 141 1.05.04, 141 1.07.02, 141 1.07.04, 141 1.07.05, 141 1.07.06, 141 1.08.01, 141 1.08.04, 141 1.10.02, 141 1.10.04, 141 1.10.05, 141 1.10.06, 141 1.10.09, 141 1.10.10, 141 1.11.07, 141 1.11.08, 141 1.13.01, 141 1.13.02, 141 1.13.03, 141 1.13.04, 141 1.13.05
2a	141 1.01.05, 141 1.08.04
2b-f	141 1.01.05
3a	141 1.06.01, 141 1.06.02, 141 1.08.01, 141 1.08.03, 141 1.13.07
3b	141 1.06.01, 141 1.06.02, 141 1.12.02, 141 1.12.03
4	141 1.07.01, 141 1.10.01, 141 1.13.03, 141 1.13.07
5	141 1.07.06, 141 1.08.03, 141 1.10.03, 141 1.10.14, 141 1.15.02
6	141 1.10.12, 141 1.10.13, 141 1.14.05, 141 1.14.06
7a,b	141 1.11.03
8a,b	141 1.11.03
9	141 1.11.03
10	141 1.11.03
11a-g	141 1.11.04
12a-c	141 1.11.04
13a-d	141 1.11.04
14	141 1.11.02
15	141 1.11.06
16	141 1.11.08
17	141 1.11.06
18	141 1.08.04
19a	141 1.04.05, 141 1.04.06, 141 1.15.05
19b	141 1.04.05, 141 1.04.06
20	141 1.14.02
21a-g	141 1.14.05
22a-n	141 1.14.06
23a,b	141 1.14.03, 141 1.14.07
24a-f	141 1.02.04
25	141 1.13.03
26	141 1.06.03

A1.3 Test Setup To Test ID Cross Reference. The following table lists the test cases, by Test ID, that use each of the test setups described in Section 6.3.2.

Test Setup	Test Case(s)
A	141 1.10.04, 141 1.10.05, 141 1.10.12, 141 1.10.15, 141 1.14.08, 141 1.15.01, 141 1.15.02, 141 1.15.03, 141 1.15.04
B	141 1.01.01, 141 1.01.02, 141 1.01.03, 141 1.01.04, 141 1.01.05, 141 1.01.06, 141 1.01.07, 141 1.03.01, 141 1.03.02, 141 1.03.03, 141 1.03.04, 141 1.05.01, 141 1.05.02, 141 1.05.03, 141 1.06.03, 141 1.07.01, 141 1.07.02, 141 1.07.04, 141 1.08.04, 141 1.10.02, 141 1.10.13, 141 1.11.07, 141 1.14.02
C	141 1.06.01, 141 1.06.02, 141 1.08.03, 141 1.12.02, 141 1.12.03

D	141 1.10.06, 141 1.14.03, 141 1.14.07
E	141 1.10.08, 141 1.10.10
F	141 1.10.09
G	141 1.10.1 1
H	141 1.02.04, 141 1.1 1.08
I	141 1.1 1.05
J	141 1.1 1.06
K	141 1.1 1.02, 141 1.1 1.03, 141 1.1 1.04
L	141 1.02.01, 141 1.02.02, 141 1.02.03, 141 1.02.05
M	141 1.04.01, 141 1.04.05, 141 1.04.06, 141 1.08.04
N	141 1.05.04, 141 1.07.05, 141 1.07.06, 141 1.08.01, 141 1.08.04
O	141 1.04.02, 141 1.04.03, 141 1.04.04
P	141 1.08.01
Q	141 1.10.07
R	141 1.10.01
S	141 1.1 1.01
T	141 1.10.03
U	141 1.13.01, 141 1.13.02
V	141 1.13.05
W	141 1.13.04
X	141 1.13.06, 141 1.13.07, 141 1.14.09
Y	141 1.14.04, 141 1.16.01
Z	141 1.14.05, 141 1.14.06
AA	141 1.10.14
BB	141 1.1 1.09
CC	141 1.09.01
DD	141 1.09.02
EE	141 1.13.03